MIMOS

Collaborators **Emerald Systems** Engineering Design Solutions & Services **MY TECHNOLOGY**

GREEN MOTION CONTROL IC
FOR PERMANENT MAGNET SYNCHRONOUS MOTOR

FEATURES

- **Field-oriented control**
- **Torque and velocity control**
- **PI controller with saturation and anti-windup for current and velocity loops**
- **Single 3.3V supply with on-chip 1.8V regulator for digital circuits**
- **On-chip oscillator eliminates the need for external oscillator**
- **Two on-chip 10-bit ADC for simultaneous sampling of phase A and B currents**
- **On-chip voltage references for ADC and common mode voltage**
- **Programmable PWM frequency**
- **Programmable velocity loop sampling rate**
- **On-the-fly programmable speed and torque references**
- **SPI serial interface**
- **Space vector PWM reduces output harmonic distortion and provides efficient utilisation of supply voltage**
- **Open loop field weakening allows extended motor speeds beyond nominal speed**
- **CORDIC implementation increases overall accuracy by improving the accuracy of sine and cosine computations**
- **Fully hardware implemented state machine reduces latency, thus increases accuracy**
- **Capable of estimating initial rotor position based on UVW encoder inputs, thus eliminating the need for rotor alignment upon reset**
- **40-pin, 6mm x 6mm QFN package**

APPLICATIONS

- **Machine tools**
- **Power tools**
- **Process automation**
- **Industry – compressors, pumps, blowers and centrifuges**
- **White goods – refrigerators and air conditioners**
- **Office automation – printers, plotters, photocopiers, scanners, DVD-ROM and hard disk**
- **Transportation – electric or hybrid vehicles, elevators, escalators, and aircraft flight control surface actuation**

DESCRIPTION

Green Motion Controller (MCGP02I) is a high performance, general purpose motion control IC providing field oriented control (FOC) for permanent magnet synchronous motors (PMSM). It frees the host processor for other tasks by performing all time-intensive digital signal processing (DSP) functions of the FOC. The programmability of all control parameters enables maximum flexibility and quick design of control systems. With an integrated on-chip oscillator, ADCs, voltage references and regulator, the complete control system can be constructed with minimum number of components, thus reducing the PCB real estate as well as overall system cost. A complete control system using MCGP02I can be comprised of merely a host processor to specify commands via SPI, a pair of fully differential amplifiers, a 3-phase PWM motor driver and a PMSM with incremental and UVW encoders. No other costly components like ADCs, voltage references and oscillator are necessary.
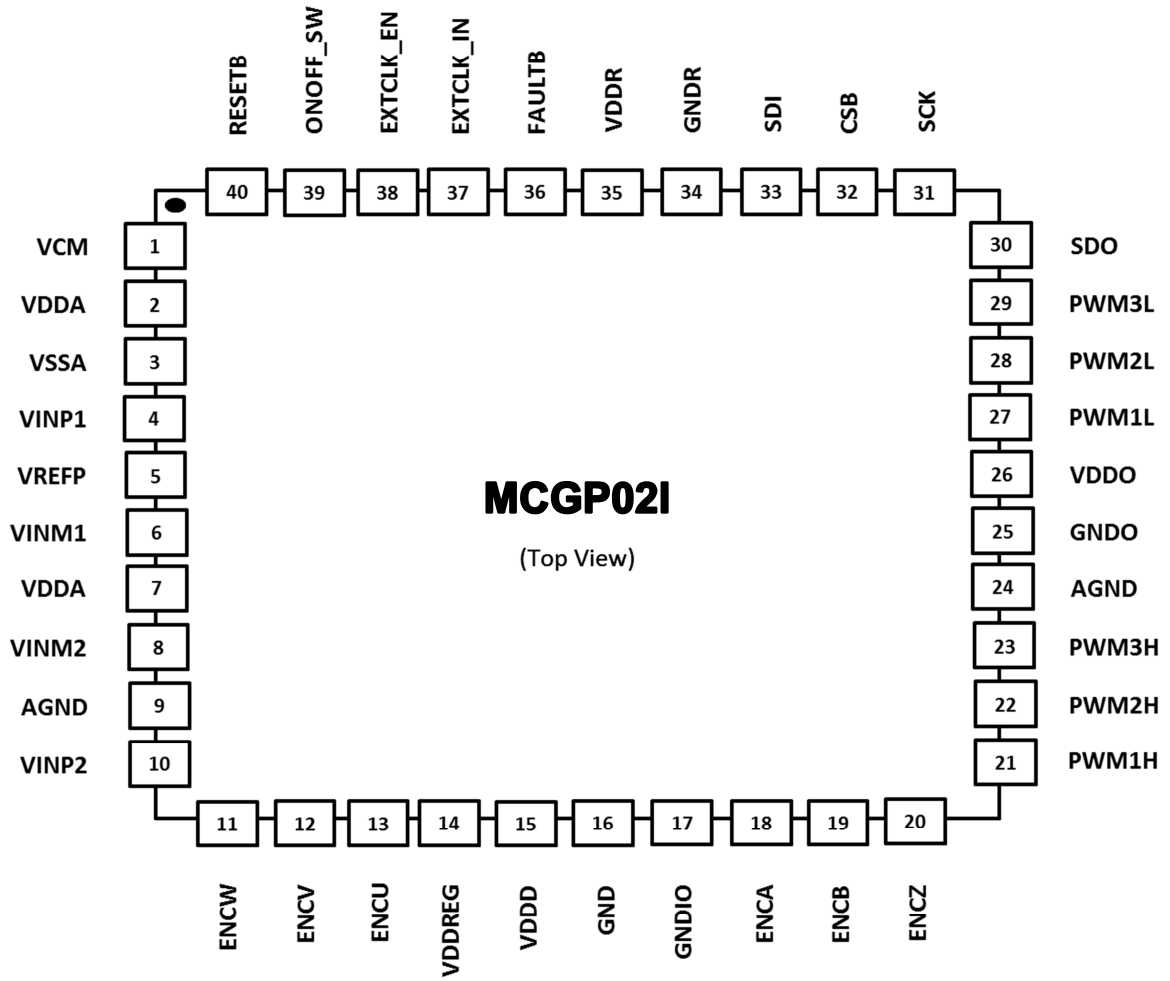
Pinout

Figure 1 - Pin Configuration

Pinout Description

SYMBOL	PIN	I/O	BUFFER	5V TOLERANT	DESCRIPTION
VCM	1	O	ANA	-	Common mode voltage
VDDA	2	I	POW	-	3.3V supply for analog circuits
VSSA	3	I	POW	-	GND for VDDA
VINP1	4	I	ANA	-	ADC1 positive input
VREFP	5	O	ANA	-	VREFP for both ADCs
VINM1	6	I	ANA	-	ADC1 negative input
VDDA	7	I	POW	-	3.3V supply for analog circuits
VINM2	8	I	ANA	-	ADC2 negative input
AGND	9	I	POW	-	GND for VDDA and substrate
VINP2	10	I	ANA	-	ADC2 positive input
ENCW	11	I	DIG(ST)	Yes	UVW Encoder input
ENCV	12	I	DIG(ST)	Yes	UVW Encoder input
ENCU	13	I	DIG(ST)	Yes	UVW Encoder input
VDDREG	14	I	POW	-	3.3V input for the on-chip 1.8V regulator
VDDD	15	I	POW	-	1.8V digital supply (internally generated)
GND	16	I	POW	-	1.8V digital GND
GNDIO	17	I	POW	-	1.8V level shifter GND
ENCA	18	I	DIG(ST)	Yes	Quadrature encoder input
ENCB	19	I	DIG(ST)	Yes	Quadrature encoder input
ENCZ	20	I	DIG(ST)	Yes	Quadrature encoder input
PWM1H	21	O	DIG	-	PWMH output
PWM2H	22	O	DIG	-	PWMH output
PWM3H	23	O	DIG	-	PWMH output
AGND	24	I	POW	-	GND for substrate
GNDO	25	I	POW	-	GND for low noise output buffer
VDDO	26	I	POW	-	3.3V supply for low noise output buffer
PWM1L	27	O	DIG	-	PWML output
PWM2L	28	O	DIG	-	PWML output
PWM3L	29	O	DIG	-	PWML output
SDO	30	O	DIG	-	SPI data output
SCK	31	I	DIG	Yes	SPI clock input
CSB	32	I	DIG	Yes	SPI chip select input
SDI	33	I	DIG	Yes	SPI data input
GNDR	34	I	POW	-	GND for low noise input buffer
VDDR	35	I	POW	-	3.3V supply for low noise input buffer
FAULTB	36	I	DIG	Yes	Fault input from motor driver (active low)
EXTCLK_IN	37	I	DIG	Yes	External clock input
EXTCLK_EN	38	I	DIG	Yes	Enable external clock and disable internal oscillator when high
ONOFF_SW	39	I	DIG	Yes	Run motor control operation
RESETB	40	I	DIG	Yes	Reset input (active low)

Remarks:

POW: Power   ST: Schmitt Trigger   ANA: Analog   DIG: Digital

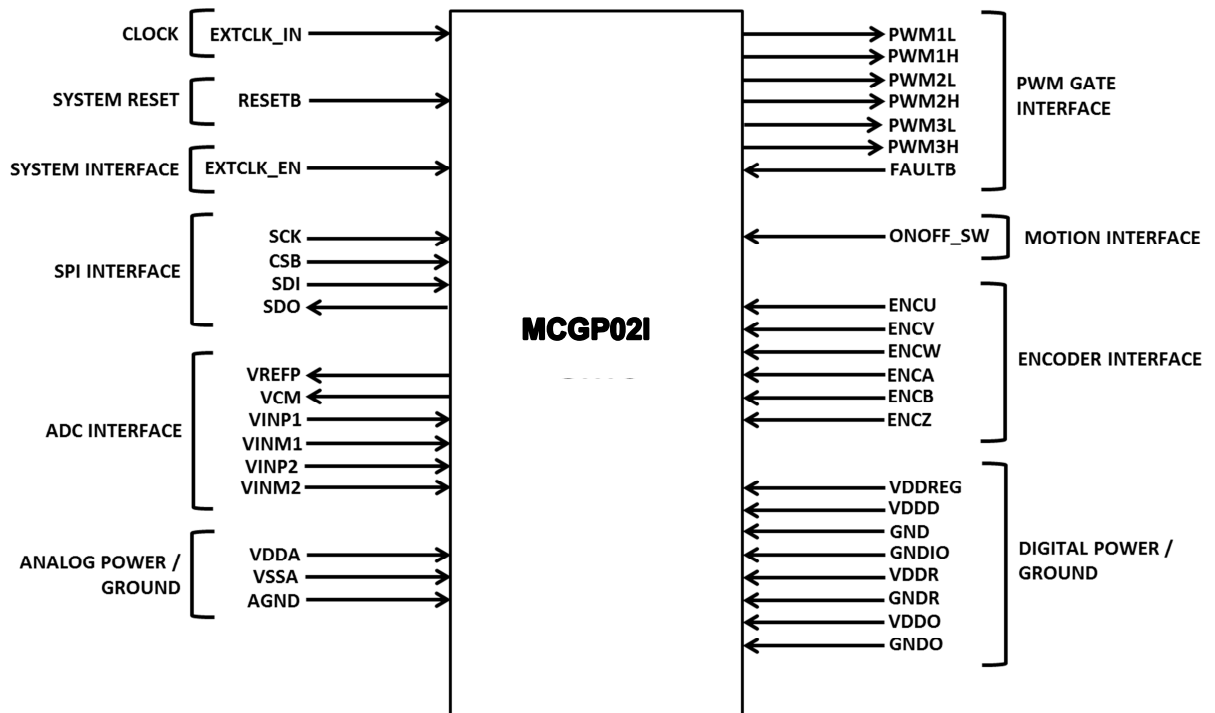## Input/Output of MCGP02I

Figure 2 - Input/Output of MCGP02I

ADC Interface

VREFP is the positive reference and VCM is the common mode voltage used by both the two internal fully differential 10 bit ADCs. The VCM pin is used to set the output common mode voltage of a fully differential amplifier. A 0.1µF capacitor must be connected to both VREFP and VCM pins referenced to VSSA.

Analog Power/Ground

VDDA is the analog power supply with reference to VSSA. VDDA is typically set to 3.3V. AGND is the IC substrate voltage and both AGND and VSSA are set to 0V.

Digital Power/Ground

VDDREG is the input for the internal regulator whose output is VDDD. VDDREG is typically set to 3.3V while the output of the regulator is 1.8V on VDDD pin. A 3.3µF tantalum capacitor (or low ESR 2.2µF electrolytic capacitor plus 100nF ceramic capacitor) must be connected to the VDDD pin which is referenced to the GND pin. VDDD will be used for all the internal logic. VDDO and VDDR are typically set to 3.3V referenced to GNDO and GNDR respectively. GND, GNDIO, GNDO, and GNDR are set to 0V.
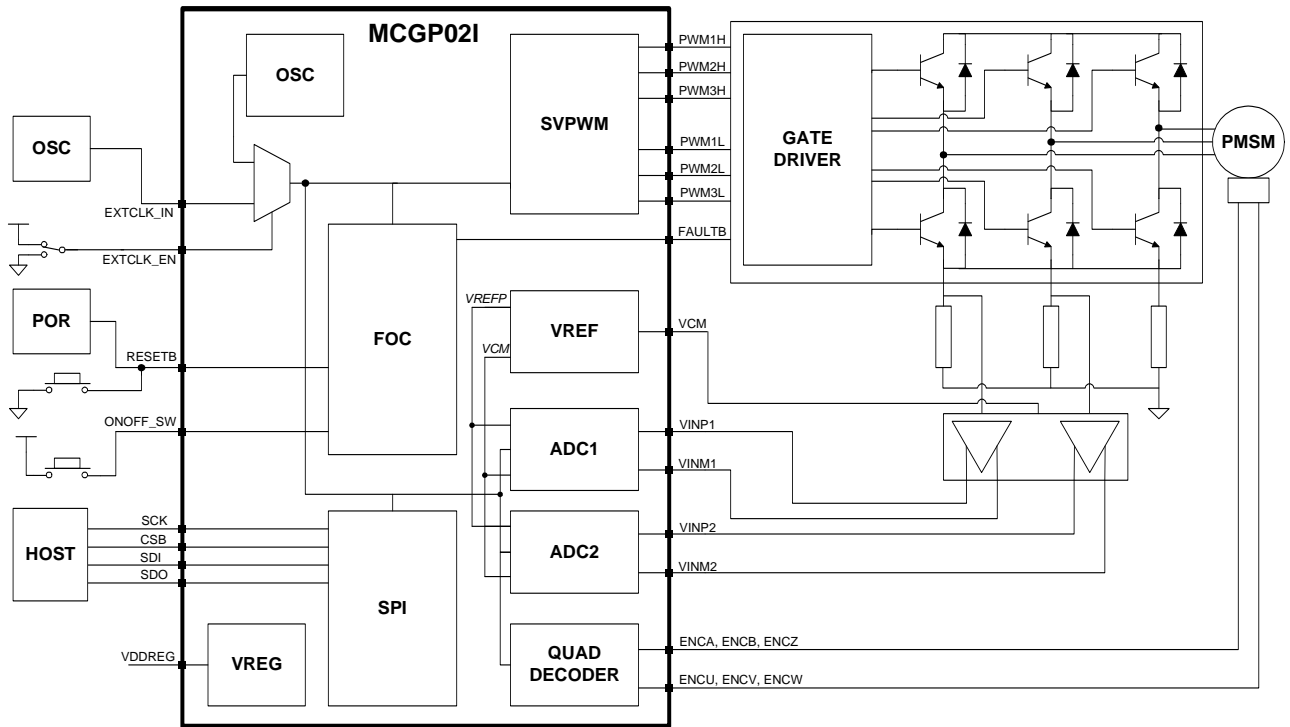
Theory of Operation
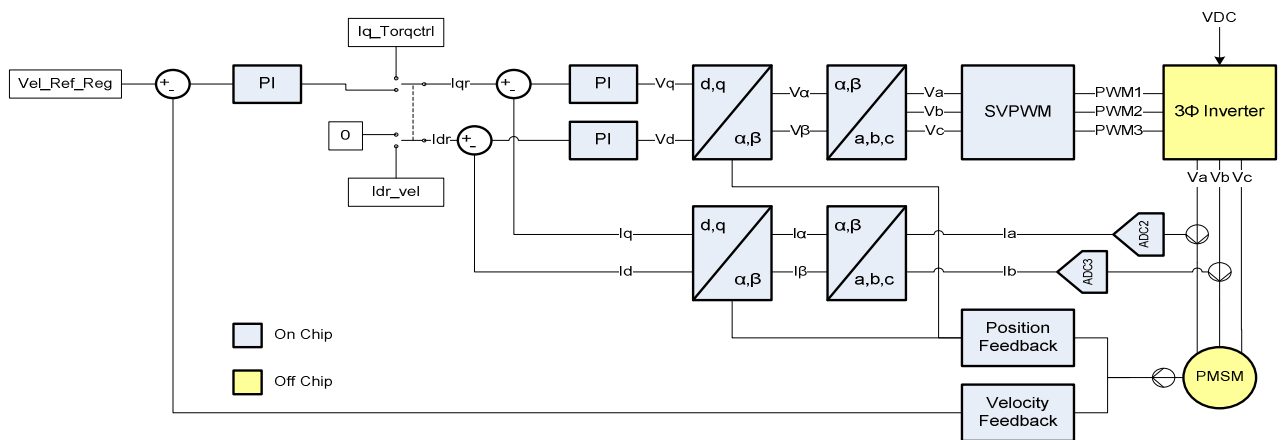

Figure 3 - Motion Control System Block Diagram

Figure 4 - Control Structure

MCGP02I offers two functional modes, namely Torque Control and Velocity Control. In Torque Control mode, MCGP02I provides users with the capability to control the driven Permanent Magnet Synchronous motor with constant torque. On the other hand, users can program MCGP02I to function in Velocity Control mode, in order to control their Permanent Magnet Synchronous motors to run in a constant targeted velocity.

Torque Control Mode

In order to run MCGP02I in torque control mode, users need to write into several Configuration Registers as listed in Table 1 via Serial Peripheral Interface (SPI) upon releasing the RESETB signal. The sequence of the SPI writing can be arbitrary, as long as bit 0 (START bit) of the Fn register and the ONOFF_SW pin are kept low. Upon completion of the SPI write onto the related registers, asserting ONOFF_SW pin or a write of 05H into the Fn register (17H) will command MCGP02I to begin operation in Torque Control mode.

During this mode of operation, the direct and quadrature current control loops will function to provide a closed loop control on the direct and quadrature currents, Id and Iq of the motor to meet the direct and quadrature reference currents (Figure 4). In this regard, the quadrature reference current, Iqr is specified in the Iq_TorqCtrl register (15H), while the direct reference current is always set to zero to ensure maximum useful torque is produced by the motor. The sampling interval for both of the current loops is similar to the PWM frequency which is defined using the Tz register (11H).

The targeted quadrature current of the running motor can be altered on-the-fly by continuously writing the targeted new values into the Iq_TorqCtrl register. The Torque Control mode allows users to pause and resume the motor without the need for a reset. This is accomplished by just de-asserting the ONOFF_SW pin or writing a '0' into bit 0 of the Fn register to pause the motor. To resume the motor, users can just assert the ONOFF_SW pin or write a '1' into bit 0 of the Fn register, without the fear of experiencing an integral kick as MCGP02I clears the integral buffer of both of the current loops whenever a pause is issued.

Velocity Control Mode

Similar to the Torque Control mode, MCGP02I requires users to write into several Configuration Registers as listed in Table 1 via SPI prior to running MCGP02I in Velocity Control mode after reset. The sequence of the SPI writing can also be arbitrary, as long as bit 0 (START bit) of the Fn register and the ONOFF_SW pin are kept low. Only upon completion of the SPI write into the related registers, asserting ONOFF_SW pin or a write of 01H into the Fn register will command MCGP02I to begin operating in Velocity Control mode.

During this mode of operation, the velocity control loop will function to provide closed loop velocity control on the PMSM motor to meet the reference velocity as provided in Vel_Ref_Reg (Figure 4). The sampling interval of this velocity control loop is defined to be a multiple of the PWM period by the Speedstep register (01H). The output of this velocity compensator is the referenced quadrature current, Iqr for the quadrature current control loop.

On the other hand, the direct current reference, Idr for the direct current control loop is supplied by Idr_vel register (16H). This way, the user can command the direct current of the PMSM motor in an open loop manner, so as to provide some degree of field weakening which will extend the velocity of the motor to exceed its nominal speed. However, this comes with an expense in the maximum and nominal torque of the commutated motor where both will be reduced in proportion to the motor speed. In doing so, care must be taken to ensure that the worst case stator current, Is does not exceed the maximum allowable stator current, I_{smax} of the motor.

$$I_s = \sqrt{I_d^2 + I_q^2} \leq I_{smax}$$

The referenced velocity in Vel_Ref_Reg register can only be updated when Status Register bit 4 = '1' so as to ensure that the new commanded velocity will be received correctly by the internal state machine. Velocity Control mode also allows users to pause and resume the motor without the need for a reset. This is accomplished by just de-asserting the ONOFF_SW pin or writing a '0' into bit 0 of the Fn register to pause the motor. To resume the motor, users can assert the ONOFF_SW pin or write a '1' into bit 0 of the Fn register, without the fear of experiencing an integral kick as MCGP02I clears all the integral buffers of the current loops and velocity loop whenever a pause is issued.

Electrical Specifications

Absolute Maximum Ratings

Operating Temperature, T_A _____ -40°C to 85°C

Storage Temperature, T_S _____ -55°C to 125°C

Supply Voltage, V_{DA} _____ -0.3V to 3.6V

Digital Input Voltage, V_{DIG} _____ -0.3V to 5V

Maximum Operating Clock Frequency, f_{CLK} _____ 20MHz

Electrical Characteristics

V_{DA}; V_{DDA}, V_{DDO}, V_{DDR}, V_{DDREG} = 3.0V to 3.6V; T = -40°C to 85°C.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
Power Supply						
1. Supply Voltage	V_{DA}	3.0	3.3	3.6	V	V_{DDA}, V_{DDO}, V_{DDR}, V_{DDREG}
2. Supply Current i) Operating	ID_{ACTIVE}			7.8	mA	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
ii) Idle	ID_{STDBY}			3.7	mA	EXTCLK_EN= High
3. Power Dissipation	P_D			28.1	mW	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
Digital Inputs CMOS						
4. Input Low Voltage	V_{IL}			0.3V_{DDR}	V	3V≤ V_{DDR} ≤3.6V
5. Input High Voltage	V_{IH}	0.7V_{DDR}			V	3V≤ V_{DDR} ≤3.6V
6. Input Leakage Current	I_{IL}	-1		1	µA	T = -40°C to 85°C, V_{DDR}= 3V to 3.6V
7. Input Capacitance	C_{IN}		1.5		fF	
Digital Inputs Schmitt Trigger						
8. Positive Schmitt Threshold	V_{TH+}			2.4V	V	3V≤ V_{DDR} ≤3.6V
9. Negative Schmitt Threshold	V_{TH-}	0.8			V	3V≤ V_{DDR} ≤3.6V
10. Input Leakage Current	I_{IL}	-1		1	µA	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
11. Input Capacitance	C_{IN}		1.5		fF	
Digital Outputs						
12. Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2 mA
13. Output High Voltage	V_{OH}	0.8V_{DDO}			V	I_{OH} = 2 mA
14. Output Capacitance	C_{OUT}		1		fF	
15. Capacitive Loading	C_{LOUT}		25		pF	
Analog Inputs						
16. Input Voltage Range	V_{INP}-V_{INM}	0		V_{REFP}	V	
17. Input Resistance	R_{INA}		150		Ω	During acquisition phase
18. Input Capacitance	C_{INA}			32.8	pF	During acquisition phase
Internal Voltage Reference						
19. High Reference Voltage	V_{REFP}	2.47		2.56	V	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
20. Low Reference Voltage	V_{REFN}		0		V	
21. Common-Mode Voltage	V_{CM}	1.23		1.28	V	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
Analog To Digital Conversion						
22. Resolution	N_R			10	bits	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
23. Integral Non-Linearity	INL			±1.3	LSB	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
24. Differential Non-Linearity	DNL			±1	LSB	T = -40°C to 85°C, V_{DA}= 3V to 3.6V No missing code
25. Gain Error	ERR_G			±1.5	LSB	T = -40°C to 85°C, V_{DA}= 3V to 3.6V
26. Offset Error	ERR_O			±1.6	LSB	T = -40°C to 85°C, V_{DA}= 3V to 3.6V

Analog and Timing Characteristics

V_{DA}; V_{DDA}, V_{DDO}, V_{DDR}, V_{DDREG} = 3.0V to 3.6V; T_A = -40°C to 85°C.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITION
External Clock Input						
27. Clock Frequency	f_{CLK}	2		20	MHz	
28. Pulse Width, Clock High	t_{CpWH}			25	ns	At 50% V_{DA} level, Clock freq=20MHz
29. Pulse Width, Clock Low	t_{CPWL}			25	ns	At 50% V_{DA} level, Clock freq=20MHz
30. Clock Rise Time	t_{CR}			3	ns	
31. Clock Fall Time	t_{CF}			3	ns	
Internal Oscillator						
32. Oscillator Frequency	f_{OSC}	18		20	MHz	
Reset						
33. Power-On Reset Delay	t_{RP}	200			us	
34. Out of Reset Delay	t_{RH}	10			us	
Digital I/O						
35. Input Rise/ Fall Time	t_{INRF}			5	ns	
36. Output Rise/ Fall Time	t_{OUTRF}		6		ns	C_{LOAD} 25pF
SPI						
37. SCK Frequency	f_{SCK}			10	MHz	SCK ≤ ½ f_{CLK}
38. SCK High Time	t_{SCKH}		50		ns	
39. SCK Low Time	t_{SCKL}		50		ns	
40. SCK Rise and Fall Time	t_{SCKRF}			5	ns	SCK = 10MHz
41. CSB↓ to SCK↑	$t_{CSL2SCH}$	50			ns	
42. SCK↓ to CSB↑	$t_{CSH2SCL}$	50			ns	
43. CSB Rise and Fall Time	t_{CSRF}			5	ns	SCK = 10MHz
44. CSB High Time	t_{CSH}	50			ns	
45. CSB High Time (Data Phase)	t_{CSHD}	50			ns	
46. SDI Data Setup Time	$t_{SDISETUP}$	1			ns	
47. SDI Data Hold Time	$t_{SDIHOLD}$	50			ns	
48.SDO Data Valid	$t_{SCL2DOV}$			45	ns	
PWM						
49. PWM Period	t_{PWMPER}			$2046t_{CPER}$	ns	t_{CPER} = 1/ f_{CLK}
50. PWM Pulse Width	t_{PWMPW}		0.5 t_{PWMPER}		ns	

Note: Clock Domain Crossing (CDC) implementation of two flops is implemented on the SPI incoming signals of SCK, SDI, CSB thus accounting for CDC issues.
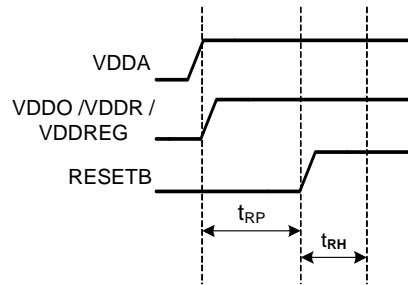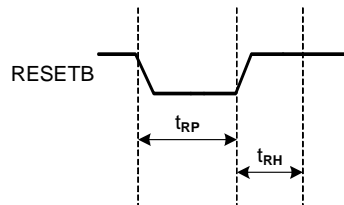
Write Cycle
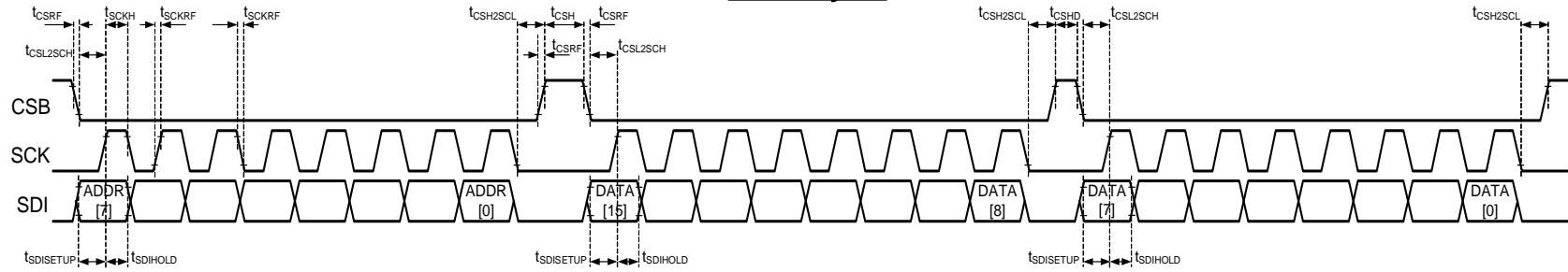
Read Cycle
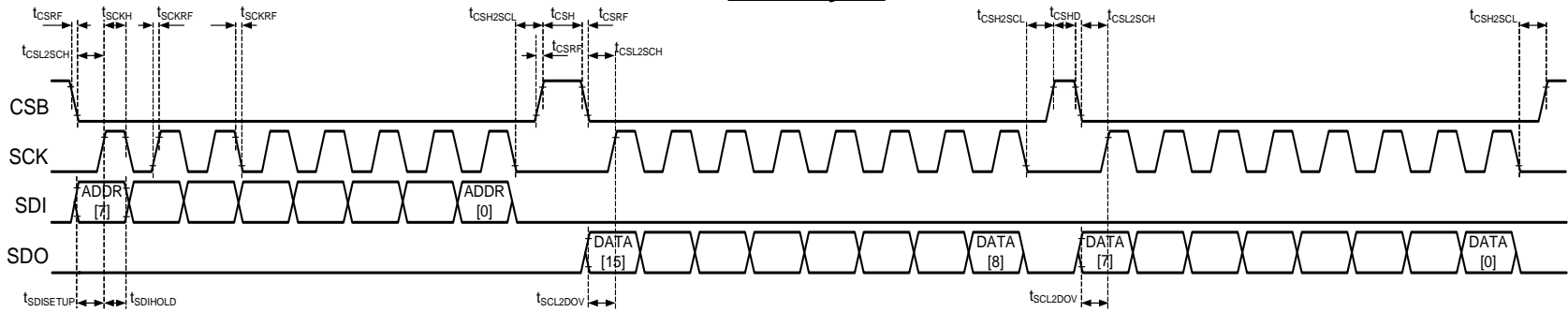
Reset Timing Diagrams

Power On Reset Sequence

VDDA

VDDO /VDDR /
VDDREG

RESETB

t_{RP}

t_{RH}

Hard Reset

RESETB

t_{RP}

t_{RH}

Configuration Registers

Table 1

ADDRESS (HEX)		REGISTER NAME	OPERATING MODE	DATA FORMAT
READ	WRITE			
01	81	Speedstep	Velocity Ctrl	Q15.0
02		Reserved – Must be at value 0000H		
03		Reserved – Must be at value 0000H		
04	84	Kvel	Velocity Ctrl	Q0.15
05	85	Kenc	All	Q0.15
06	86	Kcur	All	Q3.12
07	87	Iqrlimit	Velocity Ctrl	Q3.12
08	88	Vmax	All	Q3.12
09	89	Vmin	All	Q3.12
0A	8A	Kp	Velocity Ctrl	Q7.8
0B	8B	Ki	Velocity Ctrl	Q7.8
0C	8C	Kc	Velocity Ctrl	Q3.12
0D	8D	Kpid	All	Q7.8
0E	8E	Kiid	All	Q7.8
0F	8F	Kcid	All	Q3.12
10	90	Enc_Res	All	Q15.0
11	91	Tz	All	Q10.0
12	92	TzOverVDC	All	Q11.4
13	93	MaxDuty	All	Q10.0
14	94	Tdead	All	Q7.0
15	95	Iq_TorqCtrl	Torque Ctrl	Q3.12
16	96	Idr_vel	Velocity Ctrl	Q3.12
17	97	Fn	All	Scalar
18		Status	All	Scalar
19	99	Vel_Ref_Reg	Velocity Ctrl	Q3.12
1A	9A	IrefOn_Count	All	Q15.0
1B	9B	Initpos0	All	Q15.0
1C	9C	Initpos1	All	Q15.0
1D	9D	Initpos2	All	Q15.0
1E	9E	Initpos3	All	Q15.0
1F	9F	Initpos4	All	Q15.0
20	A0	Initpos5	All	Q15.0
21	A1	Initpos6	All	Q15.0
22	A2	Initpos7	All	Q15.0
23	A3	ActposP0	All	Q15.0
24	A4	ActposP1	All	Q15.0
25	A5	ActposP2	All	Q15.0
26	A6	ActposP3	All	Q15.0
27	A7	ActposP4	All	Q15.0
28	A8	ActposP5	All	Q15.0
29	A9	ActposP6	All	Q15.0
2A	AA	ActposP7	All	Q15.0
2B	AB	PosCalMode	All	Scalar
2C	AC	EncZMarkP	All	Q15.0

Table 1 – cont'd

ADDRESS (HEX)		REGISTER NAME	OPERATING MODE	DATA FORMAT
READ	WRITE			
2D	AD	EncZMarkN	All	Q15.0
2E	AE	GainCor1	All	Q7.8
2F	AF	GainCor2	All	Q7.8
30	B0	Offset1	All	Q10.0
31	B1	Offset2	All	Q10.0
32		Reserved – Must be at value 0000H		
33		Reserved – Must be at value 0000H		
34	B4	ActposN0	All	Q15.0
35	B5	ActposN1	All	Q15.0
36	B6	ActposN2	All	Q15.0
37	B7	ActposN3	All	Q15.0
38	B8	ActposN4	All	Q15.0
39	B9	ActposN5	All	Q15.0
3A	BA	ActposN6	All	Q15.0
3B	BB	ActposN7	All	Q15.0
3C	BC	Kpiq	All	Q7.8
3D	BD	Kiiq	All	Q7.8
3E	BE	Kciq	All	Q3.12

Remark: Addresses 0x01H through 0x3EH are 16-bit data registers
During SPI write, unused bits should be set to 0
All register values are coded in hex

Configuration Register Description

Speedstep Register (01H)

Speedstep register is a read/write register, wherein it defines the sampling frequency for the velocity control loop in an integer multiple of the PWM period as shown below. Although the Speedstep data is in Q15.0, it works only with positive values.

$$Speedstep = {f_{PWM}}\Big/{f_{vel\_loop}}$$

Kvel Register (04H)

Kvel register allows users to define the coefficient which is used to transform the number of quadrature encoder steps captured per speedstep into the per unit velocity before feeding back into the velocity control loop. In order to minimise error as a result of fixed point computation, Kvel has to be within the following range: $32 \leq K_{vel} < 32768$

$$K_{vel} = \frac{60(2^{15})}{4(Encoder\ Resolution)(Speedstep)(^{2Tz}\!/_{f_{clk}})(Motor\ Nominal\ Speed)}$$

Kenc Register (05H)

Being a read/write register, Kenc is multiplied with the quadrature encoder count to obtain the theta of the rotor. Kenc accepts positive values only.

$$K_{enc} = (N_{pole}/Encoder\ Resolution)(2^{15})$$

Kcur Register (06H)

Kcur is the coefficient to transform the raw ADC values into the meaningful phase A and phase B per unit currents. $I_{ADC(max)}$ refers to the maximum phase current flowing in the sense resistor. $I_{MOTORnom}$ is the rated peak motor current. Kcur accepts positive values only.

$$K_{cur} = \frac{I_{ADC(max)}}{(512)(\sqrt{2})(I_{MOTORnom})}(2^{12})$$

Iqrlimit Register (07H)

Through this register, users specify the maximum per unit referenced quadrature current, Iqr that can be attained by the velocity compensation loop. Thereafter, the output of the compensation filter will be saturated at this value. Only positive values are allowed.

Vmax Register (08H)

Vmax specifies the maximum positive compensation output allowed for both the current loops. Thereafter, the output of the compensation filters will be saturated at this value.

Vmin Register (09H)

Vmin specifies the minimum compensation output allowed for both the current loops. Thereafter, the output of the compensation filters will be saturated at this value. Only negative values are allowed.

Kp Register (0AH)

Kp specifies the Proportional constant of the velocity PI control loop. Hence, Kp accepts positive values only. Refer to Figure 5 for more information.

Ki Register (0BH)

Ki specifies the Integral constant of the velocity PI control loop. Hence, Ki accepts positive values only. Refer to Figure 5 for more information.

Kc Register (0CH)

Kc specifies the integral correction constant of the velocity PI control loop. Refer to Figure 5 for more information.
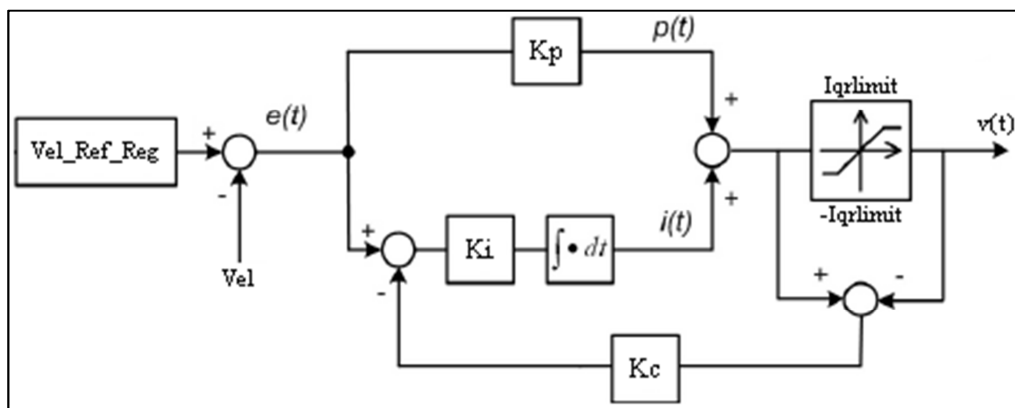
$$Kc = {Ki}/{Kp}$$

Figure 5 - MCGP02I Velocity Regulator

Kpid Register (0DH)

Kpid specifies the Proportional constant of the I_d PI control loop. Kpid accepts positive values only. Refer to Figure 6 for more information.

Kiid Register (0EH)

Kiid specifies the Integral constant of the I_d PI control loop. Kiid accepts positive values only. Refer to Figure 6 for more information.

Kcid Register (0FH)

Kcid specifies the integral correction constant of the I_d PI control loop. Refer to Figure 6 for more information.
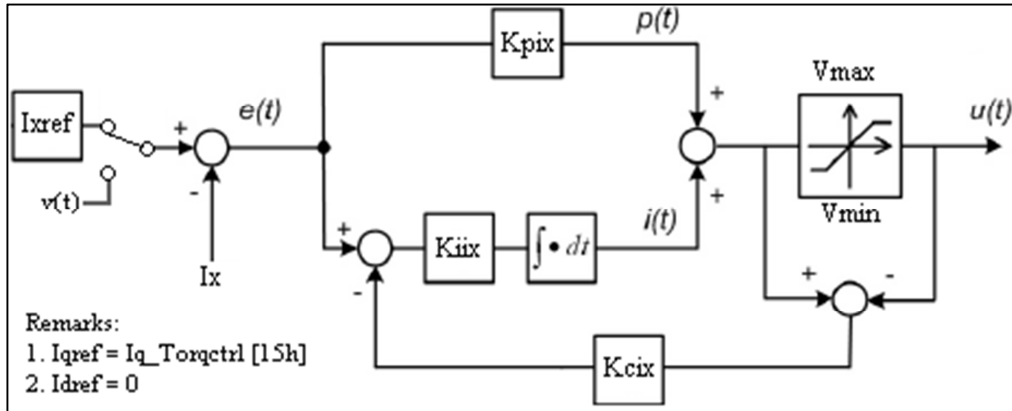
$$Kcid = {Kiid}/{Kpid}$$

Figure 6 - MCGP02I Id/Iq Current Regulators

Enc_Res Register (10H)
Enc_Res specifies the number of encoder pulses per revolution (cpr). Only positive values are allowed.

Tz Register (11H)
Tz indicates the period of the centre aligned PWM by allowing users to define the number of system clock in a half PWM period. Tz is the ratio of the system clock frequency divided by 2 times the PWM frequency. Refer to Figure 7 for more information. The value of Tz has to be within this range: $100 =< Tz < 1024$

TzOverVDC (12H)
The value of TzOverVDC is shown below. VDC is the operating voltage of the motor. Positive values are only accepted. Ke is the BEMF constant of the motor.

$$TzOverVDC = \frac{Tz(Ke)(Motor\ Nominal\ Speed)(\sqrt{2})}{VDC}(2^4)$$

MaxDuty Register (13H)
Specifies the maximum ON time for the PWM by capping the (T1 + T2) time of the Space Vector Modulation. If (T1 + T2) > MaxDuty, then T1 and T2 will be scaled accordingly so that (T1 + T2) = MaxDuty. MaxDuty accepts positive values only. The MaxDuty value is a percentage of Tz. T1 and T2 can be found in Figure 7.

Tdead Register (14H)
Specifies the dead time between the PWMH and PWML of the half bridge in terms of the number of system clock cycles. The specified dead time will be inserted into all the transitions in the PMWH and PWMLs. Tdead must be positive and non-zero. Refer to Figure 7 for more information.
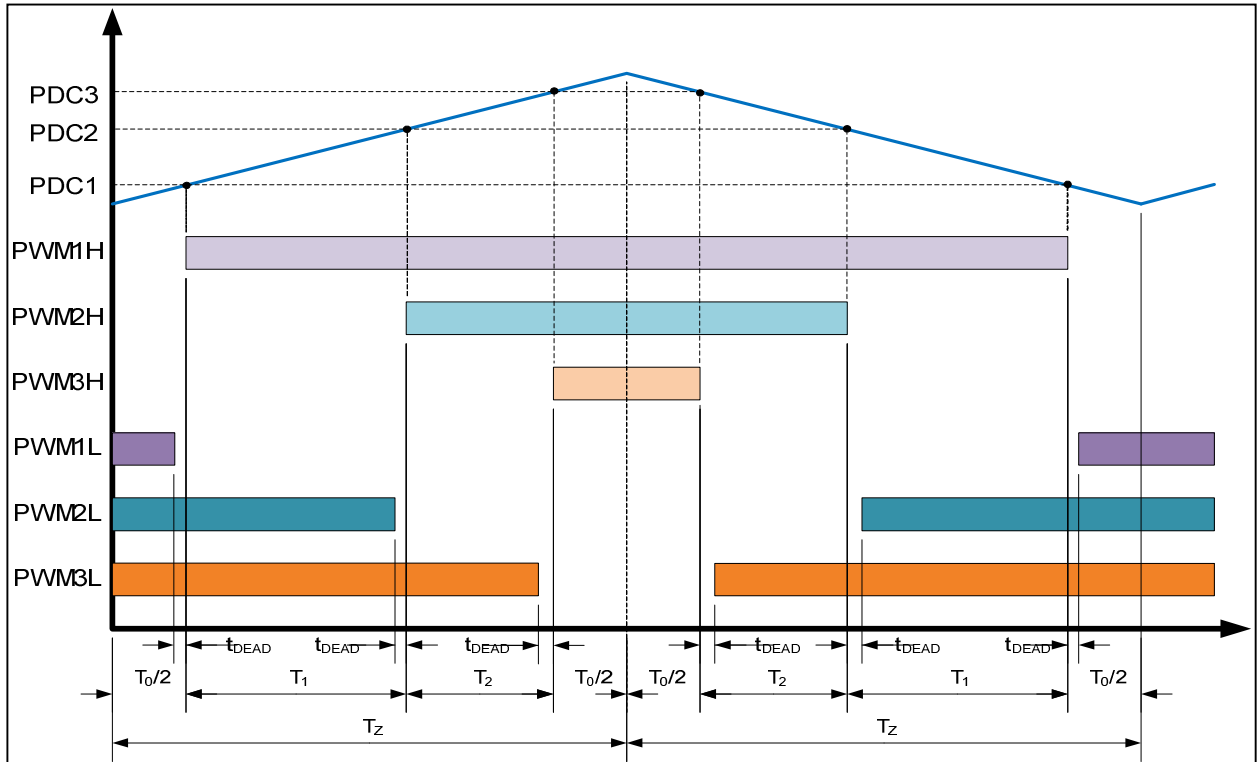
Figure 7 - MCGP02I PWM Timing Diagram

Iq_TorqCtrl Register (15H)

Specifies the per unit quadrature current reference for Torque Control mode. I_{qref} is the user required current to obtain a specific torque. I_{qnom} is the rated motor current.

$$Iq_{TorqCtrl} = \frac{Iq_{ref}}{Iq_{nom}}(2^{12})$$

Idr_vel Register (16H)

Specifies the per unit direct current reference to be used during Velocity Control mode. Hence, it can be leveraged to achieve some degree of field weakening.

Fn Register (17H)

A function register whose bits control the following:

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit 15							Bit 8

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	TORQVEL	X	START
Bit 7							Bit 0

Legend: X – Don't care

Bit 2	TORQVEL: Torque Control mode or Velocity Control mode
	When TORQVEL = 1, MCGP02I is in Torque Control mode
	When TORQVEL = 0, MCGP02I is in Velocity Control mode
Bit 0	START: Start or stop the motor
	When START = 1, MCGP02I starts the motor
	When START = 0, MCGP02I stops the motor

Status Register (18H)

Status register is a read-only register providing status during motor operation.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit 15							Bit 8

R	R	R	R	R	R	R	R
X	X	FAULT	VLCTREF	VLCT	TRQ	X	START
Bit 7							Bit 0

Legend: X – Don't care

Bit 5	FAULT: Fault status
	1 = Fault has occurred and all PWMXx will go low
	0 = Fault has not occurred
Bit 4	VLCTREF: Velocity Reference status
	1 = Vel_Ref_Reg can be updated with a new value
	0 = Internal state machine busy and Vel_Ref_Reg should not be updated
Bit 3	VLCT: Velocity Control mode status
	1 = MCGP02I is in Velocity Control mode
	0 = MCGP02I is not in Velocity Control mode
Bit 2	TRQ: Torque Control mode status
	1 = MCGP02I is in Torque Control mode
	0 = MCGP02I is not in Torque Control mode
Bit 0	START: Motor operation mode status
	1 = Motor operation started
	0 = Motor operation stopped

Vel_Ref_Reg (19H)
Specifies the per unit velocity reference. Reference Velocity is the user required revolution per minute (rpm).

$$Vel\_ref\_reg = \frac{Reference\ Velocity}{Motor\ Nominal\ Speed}(2^{12})$$

IrefOn_Count (1AH)
This is a critical register which must be filled. It specifies the number of system clocks to wait after RESETB pin goes high, before ADC acquisition is allowed. Refer to the value t_{RH}. Only positive values are allowed.

Initpos0 ~ Initpos7 Registers (1BH ~ 22H)
Specifies the estimated initial rotor position based on each of the 6 ENCU, ENCV and ENCW combinations, in terms of the absolute quadrature encoder counts. The two unused ENCU, ENCV and ENCW combinations must be programmed as zero.

ActposP0 ~ ActposP7 Registers (23H ~ 2AH)
Specifies the actual position of the rotor when rotating in the positive direction. It is based on the newly transitioned ENCU, ENCV and ENCW combinations. The values are of the absolute quadrature encoder counts. The two unused combinations shall be programmed as zero.

PosCalMode Register (2BH)
Specifies the position calibration mode used in the position feedback block prior to the first time assertion of ENCZ pin.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	X
Bit 15							Bit 8

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X	X	X	X	X	X	X	POSCAL
Bit 7							Bit 0

Legend: X - Don't care

	POSCAL : Position Calibration
Bit 0	1 = Not referencing ENCU, ENCV, ENCW
	0 = Based on ActposP/ActposN registers with reference to ENCU, ENCV, ENCW

EncZMarkP Register (2CH)
Allows users to specify the number of absolute quadrature encoder counts to the actual rotor "Zero" position upon assertion of the ENCZ, when rotating from the positive direction.

EncZMarkN Register (2DH)
Specifies the number of absolute quadrature encoder counts to the actual rotor "Zero" position upon assertion of the ENCZ, when rotating from the negative direction.

GainCor1 Registers (2EH) / Offset1 Registers (30H)
Specifies the gain corrections and offset corrections for ADC_1 respectively.
$ADC_1 = (ADC_1 + Offset_1)(GainCor_1)$

GainCor2 Registers (2FH) / Offset2 Registers (31H)

Specifies the gain corrections and offset corrections for ADC_2 respectively.

$ADC_2 = (ADC_2 + Offset_2)(GainCor_2)$

ActposN0~ActposN7 Registers (34H~3BH)

Specifies the actual position of the rotor when rotating in negative direction based on the newly transitioned ENCU, ENCV and ENCW combinations. The values are of the absolute quadrature encoder counts. The two unused combinations shall be programmed as zero.

Kpiq Register (3CH)

Kpiq specifies the Proportional constant of the I_q PI control loop. Kpiq accepts positive values only. Refer to Figure 6 for more information.

Kiiq Register (3DH)

Kiiq specifies the Integral constant of the I_q PI control loop. Kiiq accepts positive values only. Refer to Figure 6 for more information.
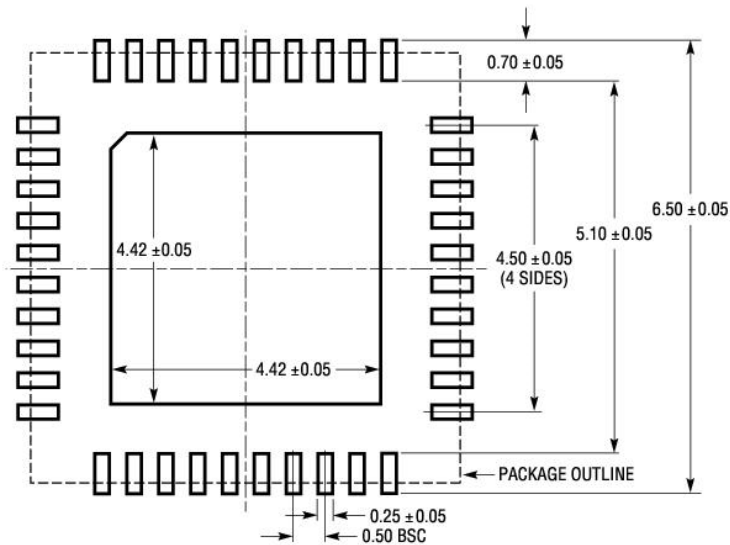
Kciq Register (3EH)

Kciq specifies the integral correction constant of the I_q PI control loop. Refer to Figure 6 for more information.
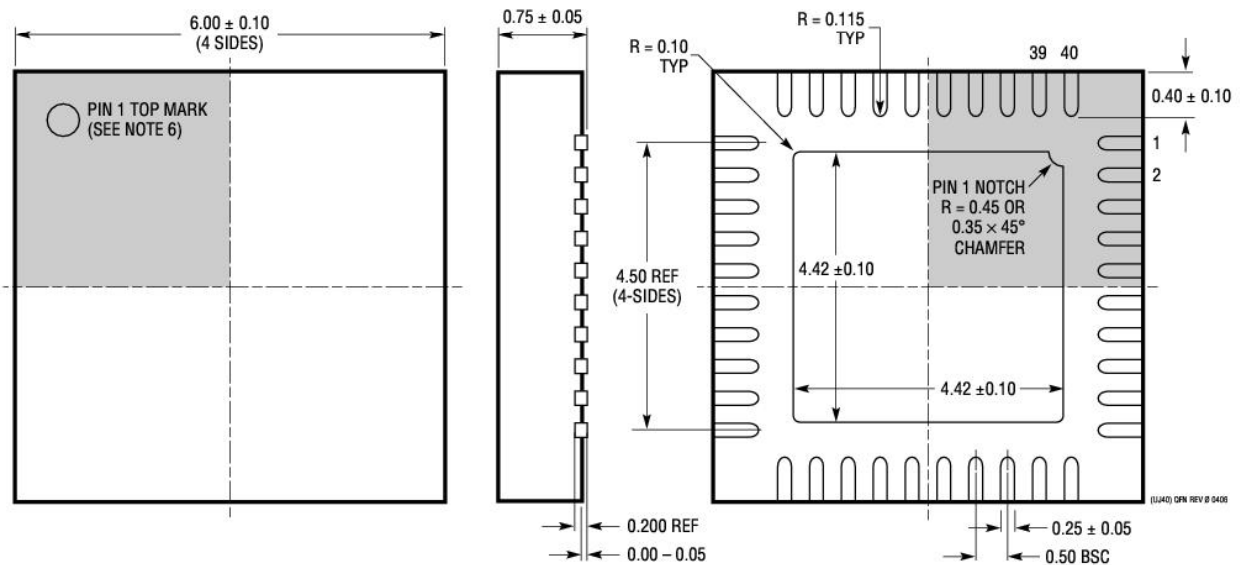
$$Kciq = {Kiiq}/{Kpiq}$$

Package Dimensions

40-Pin Plastic Quad Flat, No-Leads Package – 6mm x 6mm Body (QFN)

0.70 ±0.05

6.50 ±0.05

5.10 ±0.05

4.42 ±0.05

4.50 ±0.05
(4 SIDES)

4.42 ±0.05

PACKAGE OUTLINE

0.25 ±0.05
0.50 BSC

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

6.00 ± 0.10
(4 SIDES)

0.75 ± 0.05

R = 0.115
TYP

R = 0.10
TYP

39   40

0.40 ± 0.10

1

2

PIN 1 TOP MARK
(SEE NOTE 6)

4.50 REF
(4-SIDES)

PIN 1 NOTCH
R = 0.45 OR
0.35 × 45°
CHAMFER

4.42 ±0.10

4.42 ±0.10

(UJ40) QFN REV Ø 0406

0.200 REF

0.00 – 0.05

0.25 ± 0.05

0.50 BSC

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Revision History

Date	Remarks
6 Feb 2014	Initial Draft
27 Feb 2014	Added in initial parameters for datasheet table
3 Mar 2014	Updated parameters for datasheet table
11 Mar 2014	Updated parameters for SPI
13 Mar 2014	Updated parameters for clock oscillator
17 Mar 2014	Updated parameters for SPI and clock oscillation
18 Mar 2014	Updated clock duty cycle parameters
20 Mar 2014	Updated timing diagrams
28 Oct 2014	Initial internal release of datasheet
16 Feb 2015	Release of datasheet with MCGP02I
7 Apr 2015	Prelim - Updated configuration register layout/formulas
4 Aug 2015	Prelim - Updated pin description, specs, figures and description