AI KNN Classification SoftIP & FPGA IP Datasheet

Version 1.0

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AIRIS LABS SDN BHD (202001015529)

I2U building, Sains@USM

10, Persiaran Bukit Jambul,

11900 Bayan Lepas,

Penang, Malaysia

Tel: +6 (04) 611 6693

Email: sales@airislabs.my

www.airislabs.my

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Date	Comments
15th Sept 2020	Version 1 of datasheet
29th Sept 2020	Updated power consumption from silicon characterization
29th Oct 2020	Updated with FPGA IP information
19th Jan 2021	Updated with MAX10, Cyclone5, Cyclone10 FPGA IP information
15th April 2021	Updated for 1Mbytes Learning Data of 1024 samples with 1024 attributes for Intel Devices
13th May 2021	Updated for 1Mbytes Learning Data of 1024 samples with 1024 attributes for Xilinx Devices

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1 Introduction

AI KNN Classification SoftIP & FPGA IP is a low cost, low power consumption, high performance, general purpose KNN algorithm that is silicon proven on FPGA and TSMC 40nmLP process utilizing full logic gates and SRAM memory. Its complete KNN implementation does not require any software or programming code as the KNN algorithm is implemented as logic gates thus allowing for a very fast KNN learning and classification. It allows for a range of K values from 1 to 15 for KNN classification. It can quickly learn from 1024 samples of data with each data having a maximum of 1024 attributes allowing for 1Mbyte of learning data. AI KNN Classification comes in SoftIP and FPGA IP with different options for users to choose from:

a. Soft IP with option of
    a. max 1 Mbyte of learning data of 1024 samples with 1024 attributes per sample
    b. max 2 Mbyte of learning data of 2048 samples with 1024 attributes per sample
    c. max 4 Mbyte of learning data of 4096 samples with 1024 attributes per sample
b. FPGA IP with option
    a. max 1 Mbyte of learning data of 1024 samples with 1024 attributes per sample
    b. options for smaller size of learning data to fit into smaller FPGAs is available upon request

For KNN applications that require smaller sample size or smaller attributes per sample, AI KNN Classification SoftIP & FPGA IP allows for specifying of learning data size through ROWSIZE register and attribute size through COLUMNSIZE register thus allowing for faster learning and faster classification for smaller learning data size systems. AI KNN Classification SoftIP & FPGA IP is accessed through a high speed communication of direct writing of training data using arraywe, arraydatain, arrayaddress and clock.

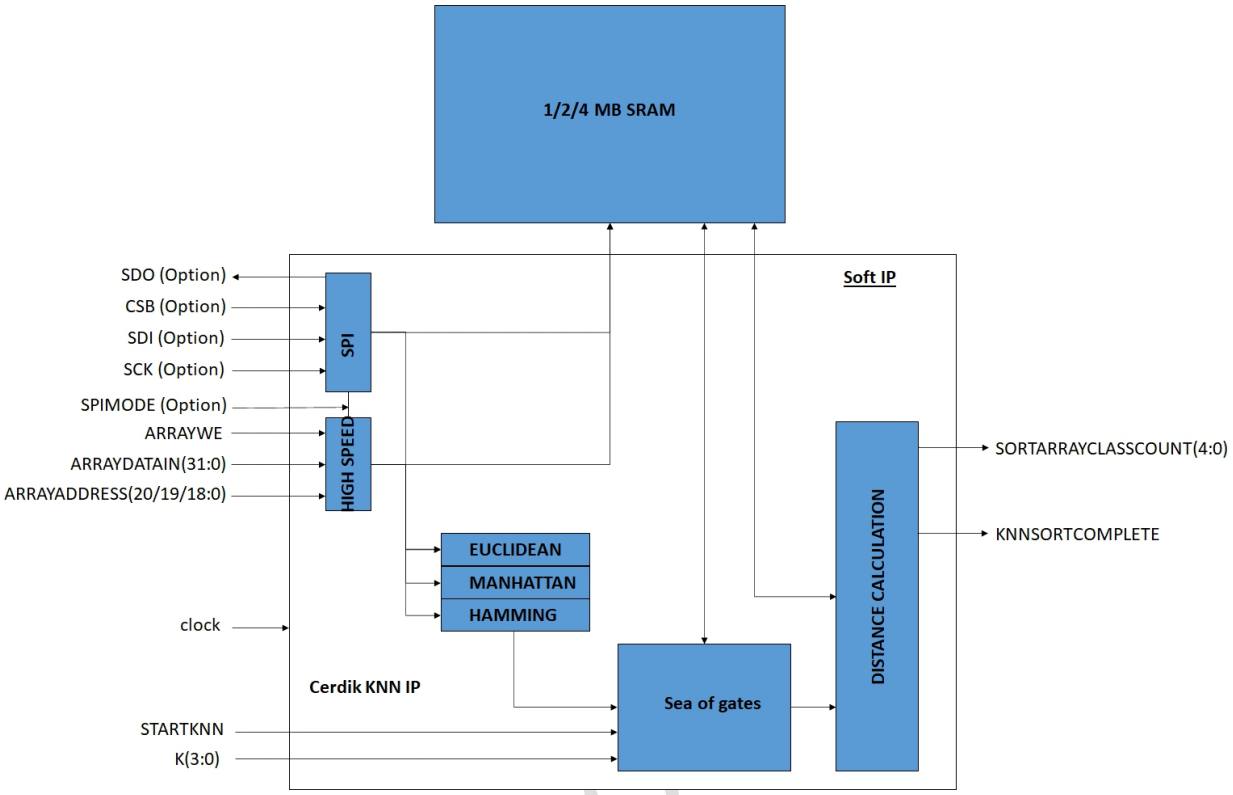


Figure 1. Top Level Block Diagram of AI KNN SoftIP

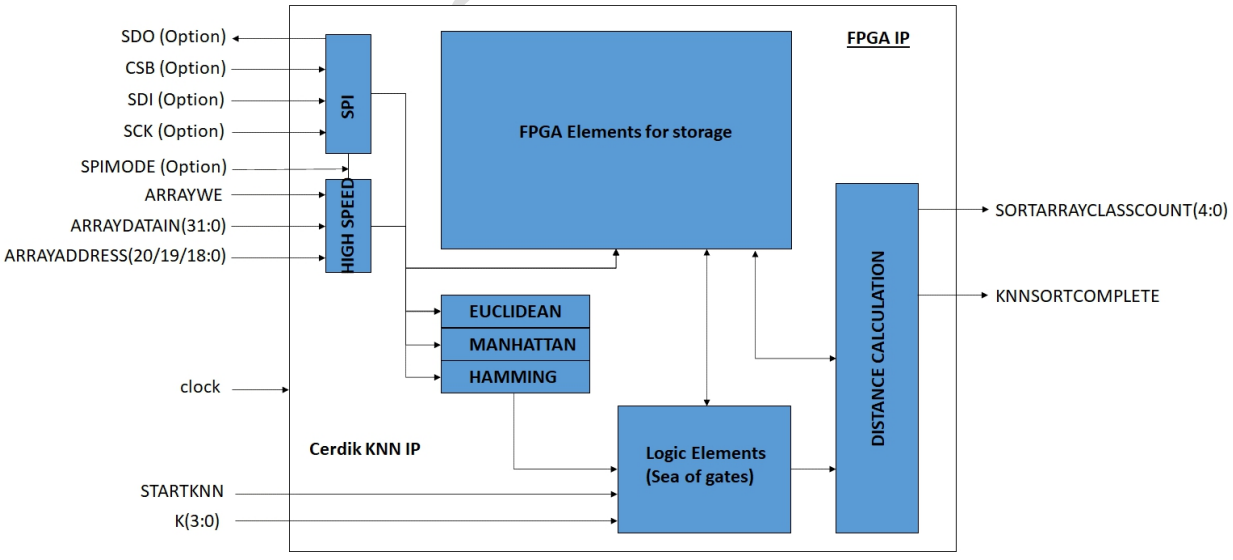


Figure 2. Top Level Block Diagram of AI KNN FPGA IP

2 Features

- Soft IP
  - KNN classification capable of 1/2/4 Mbyte of learning data
  - 1k, 2k, 4k option of samples
  - 1024 attributes per sample for learning
  - Programmable attributes size in multiples of 64
  - Programmable learning data size
    - 2 to 1024 for 1k option
    - 2 to 2048 for 2k option
    - and 2 to 4096 for 4k option
  - 19/20/21 bits arrayaddress to access learning matrix size of 1/2/4 Mbyte
  - 32 bits arraydatain to write data to learning matrix
  - Optional SPI interface
  - Programmable k value of KNN from 1 to 15
  - knnsortcomplete identifier for indication of KNN completed
  - Once learning completes, no limit to amount of KNN classification
  - Silicon proven on TSMC 40LP
- FPGA IP
  c. KNN classification capable of max 1 Mbyte of learning data with 1024 samples and 1024 attributes per sample (options for smaller size of learning data to fit into smaller FPGAs is available upon request)
  - Programmable attributes size in multiples of 64
  - 32 bits arraydatain to write data to learning matrix
  - Optional SPI interface
  - Programmable k value of KNN from 1 to 15
  - knnsortcomplete identifier for indication of KNN completed
  - Once learning completes, no limit to amount of KNN classification
  - FPGA proven

3 AI KNN Classification Silicon Proven and FPGA Proven

AI KNN Classification SoftIP 1 Mbyte learning data of 1024 samples with 1024 attributes per sample of learning data is silicon proven on TSMC40LP.

Process	Package	Package Size	Die Size	VDDIO/VCORE
TSMC40LP	QFN88	12mm x 12mm	3.848mm x 3.848mm	3.3V / 1.1V
Power consumption	0.121 W for learning 1Mbyte data of 1024 learning data with 1024 attributes per learning data and 0.144W for classification of 1 test object based on the 1 Mbyte of learned data			3.3V / 1.1V Typ
Tested on Silicon	MBIST tests	Functional tests that includes learning data and classification using the learned data		
AI KNN performance	Using iris dataset for AI classification with 10% of iris dataset as test and 90% of iris dataset for learning, classification of 100% accuracy is achieved in 16,688 clock cycles. At 100 MHz, the classification is achieved at 166.88 us (for learning 90% iris dataset and remaining 10% iris dataset for identification).			

AI KNN Classification FPGA IP 12,800 bytes of learning data with 100 samples with 128 attributes per sample of learning data is FPGA proven (options for other density of learning data to fit into different sizes of FPGAs is available upon request).

FPGA IP	FPGA	Frequency	Utilization
12,800 bytes of learning data with 100 samples of 128 attributes per sample (equivalent to 100 faces for facial recognition)	Cyclone 5 5CSXFC6D6F31C6	44 MHz	54% ALM utilization, 3% memory utilization after place and route
	Max 10 10M50DAF484C7G	29 MHz	45% logic elements utilization, 10% memory utilization after place and route
	Cyclone 10 LP 10CL055YF484C6G	45 MHz	40% logic elements utilization, 6% memory utilization after place

			and route
	Arria 5 5AGXBB1D4F31C	38 MHz	20% logic elements utilization, 1% memory utilization after synthesis before place and route
	Arria 10 10AS066H2F34E2LG	41 MHz	9% logic elements utilization, 0.5% memory utilization after synthesis before place and route
	Stratix 4 EP4SE820F43I	36 MHz	3.4% logic elements utilization, 0.6% memory utilization after synthesis before place and route
	Stratix 5 5SGSMD5H3F35C	40 MHz	13% logic elements utilization, 0.4% memory utilization after synthesis before place and route
	Stratix 10 1SX280LN3F43E1VG	60 MHz	2.5% logic elements utilization, 0.06% memory utilization after synthesis before place and route

AI KNN Classification FPGA IP 1 M Byte of learning data with 1024 samples with 1024 attributes per sample of learning data is FPGA proven on Intel devices (options for other density of learning data to fit into different sizes of FPGAs is available upon request).

FPGA IP	FPGA	Frequency	Utilization
1 MBytes of learning data with 1024 samples of 1024 attributes per sample	Cyclone 5 5CGXFC9E6F31C	26 MHz	23% ALM utilization, 68% memory utilization after place and route

	Cyclone 10 GX 10CX220YU484E5G	48 MHz	31% logic elements utilization, 71% memory utilization after synthesis before place and route
	Arria 5 5AGXBB1D4F31C	35 MHz	22% logic elements utilization, 55% memory utilization after synthesis before place and route
	Arria 10 10AS066H2F34E2LG	40 MHz	9.9% logic elements utilization, 20% memory utilization after synthesis before place and route
	Stratix 4 EP4SE820F43I	27 MHz	4% logic elements utilization, 36% memory utilization after synthesis before place and route
	Stratix 5 5SGSMD5H3F35C	39 MHz	15% logic elements utilization, 21% memory utilization after synthesis before place and route
	Stratix 10 1SX280LN3F43E1VG	58 MHz	3% logic elements utilization, 4% memory utilization after synthesis before place and route

AI KNN Classification FPGA IP 1 M Byte of learning data with 1024 samples with 1024 attributes per sample of learning data is FPGA proven on Xilinx devices (options for other density of learning data to fit into different sizes of FPGAs is available upon request).

FPGA IP	FPGA	Frequency	Utilization
1 MBytes of learning data with 1024 samples of 1024 attributes per sample	Kintex 7 xc7k160tfbg484-3	47 MHz	36% LUT, 6% FF, 75% BRAM utilization after place and route
	Zynq 7000 xa7z030fbg484-1I	35 MHz	47% LUT, 8% FF, 92% BRAM utilization after place and route
	Artix 7 xc7a200tfbg484-3	33 MHz	28% LUT, 5% FF, 67% BRAM utilization after place and route

For SoftIP, files provided for:

- Generic gate level netlist which can be optimized to any standard call library
- Integration scripts, Verilog/VHDL testbenches and datasets for verifying functionality
- Application Notes

For FPGA IP, files provided for:

- Generic gate level netlist which can be optimized to any FPGA library
- Integration scripts, Verilog/VHDL testbenches and datasets for verifying functionality
- Application Notes

4 Pin Configuration for SoftIP

Symbol	I/O	Buffer	Description
ARRAYWE	I	DIG	Write enable to write learning data to array
CLOCK	I	DIG	Clock input
ARRAYADDRESS(20/19/18:0)	I	DIG	Address for writing of learning data into array, 20: for 4k option, 19:0 for 2k option and 18:0 for 1k option
K(3:0)	I	DIG	K value for KNN
STARTKNN	I	DIG	Start the KNN algorithm for the learning data and AI classification data
KNNSORTCOMPLETE	O	DIG	KNN algorithm is complete and AI classification results valid on SORTARRAYCLASSCOUNT(4:0)
SORTARRAYCLASSCOUNT(4:0)	O	DIG	AI KNN classification result
RESETB	I	DIG	Reset, active low
SDI	I	DIG	SPI data in (Option)
SCK	I	DIG	SPI clock (Option)
CSB	I	DIG	Chip Select for SPI interface (active low) (Option)
SPIMODE	I	DIG	Enable SPI interface for writing of learning data into array (Option)
SDO	O	DIG	SPI data out (Option)
intarray1_addrA_top(16/15/14:0), intarray2_addrA_top(16/15/14:0), intarray3_addrA_top(16/15/14:0),	O	DIG	Address of portA to 8 blocks of dual port read single port write SRAM for learning data

intarray4_addrA_top(16/15/14:0), intarray5_addrA_top(16/15/14:0), intarray6_addrA_top(16/15/14:0), intarray7_addrA_top(16/15/14:0), intarray8_addrA_top(16/15/14:0)			
intarray1_datainA_top(31:0), intarray2_datainA_top(31:0), intarray3_datainA_top(31:0), intarray4_datainA_top(31:0), intarray5_datainA_top(31:0), intarray6_datainA_top(31:0), intarray7_datainA_top(31:0), intarray8_datainA_top(31:0)	O	DIG	Data to 8 blocks of dual port read single port write SRAM for learning data
intarray1_weA_top, intarray2_weA_top, intarray3_weA_top, intarray4_weA_top, intarray5_weA_top, intarray6_weA_top, intarray7_weA_top, intarray8_weA_top	O	DIG	Write enable to 8 blocks of dual port read single port write SRAM for learning data
intarray1_qA_top(31:0), intarray2_qA_top(31:0), intarray3_qA_top(31:0), intarray4_qA_top(31:0), intarray5_qA_top(31:0), intarray6_qA_top(31:0), intarray7_qA_top(31:0), intarray8_qA_top(31:0)	I	DIG	PortA readout from 8 blocks of dual port read single port write SRAM for learning data
intarray1_addrB_top(16/15/14:0),	O	DIG	Address of portB to 8 blocks of dual

intarray2_addrB_top(16/15/14:0), intarray3_addrB_top(16/15/14:0), intarray4_addrB_top(16/15/14:0), intarray5_addrB_top(16/15/14:0), intarray6_addrB_top(16/15/14:0), intarray7_addrB_top(16/15/14:0), intarray8_addrB_top(16/15/14:0)			port read single port write SRAM for learning data
intarray1_qB_top(31:0), intarray2_qB_top(31:0), intarray3_qB_top(31:0), intarray4_qB_top(31:0), intarray5_qB_top(31:0), intarray6_qB_top(31:0), intarray7_qB_top(31:0), intarray8_qB_top(31:0)	I	DIG	PortB readout from 8 blocks of dual port read single port write SRAM for learning data
intarrayclass_addrA_top(11/10/9:0)	O	DIG	Address of portA to dual port read single port write SRAM for class
intarrayclass_datainA_top(7:0)	O	DIG	Data to dual port read single port read SRAM for class
intarrayclass_weA_top	O	DIG	Write enable to dual port read single port write SRAM for class
intarrayclass_qA_top(7:0)	I	DIG	PortA readout from dual port read single port write SRAM for class
intarrayclass_addrB_out_top(11/10/9:0)	O	DIG	Address of portB to dual port read single port write SRAM for class
intarrayclass_qB_top(7:0)	I	DIG	PortB readout from dual port read single port write SRAM for class
intarraydistancepos_addrA_top(11/10/9:0)	O	DIG	Address of portA to dual port read single port write SRAM for position

intarraydistancepos_datainA_top(11/10/9:0)	O	DIG	Data to dual port read single port read SRAM for position
intarraydistancepos_weA_top	O	DIG	Write enable to dual port read single port write SRAM for position
intarraydistancepos_qA_top(11/10/9:0)	I	DIG	PortA readout from dual port read single port write SRAM for position
intarraydistancepos_addrB_out_top(11/10/9:0)	O	DIG	Address of portB to dual port read single port write SRAM for position
intarraydistancepos_qB_top(11/10/9:0)	I	DIG	PortB readout from dual port read single port write SRAM for position
intarraydistance_addrA_top(11/10/9:0)	O	DIG	Address of portA to dual port read single port write SRAM for distance
intarraydistance_datainA_top(31:0)	O	DIG	Data to dual port read single port read SRAM for distance
intarraydistance_weA_top	O	DIG	Write enable to dual port read single port write SRAM for distance
intarraydistance_addrB_out_top(11/10/9:0)	O	DIG	Address of portB to dual port read single port write SRAM for distance
intarraydistance_qA_slv_top(31:0)	I	DIG	PortA readout from dual port read single port write SRAM for distance
intarraydistance_qB_slv_top(31:0)	I	DIG	PortB readout from dual port read single port write SRAM for distance

Remarks: DIG: Digital

5 Pin Configuration for FPGA IP

Symbol	I/O	Buffer	Description
ARRAYWE	I	DIG	Write enable to write learning data to array
CLOCK	I	DIG	Clock input
ARRAYADDRESS(18:0)	I	DIG	Address for writing of learning data into array
K(3:0)	I	DIG	K value for KNN
STARTKNN	I	DIG	Start the KNN algorithm for the learning data and AI classification data
KNNSORTCOMPLETE	O	DIG	KNN algorithm is complete and AI classification results valid on SORTARRAYCLASSCOUNT(4:0)
SORTARRAYCLASSCOUNT(4:0)	O	DIG	AI KNN classification result
RESETB	I	DIG	Reset, active low
SDI	I	DIG	SPI data in (Option)
SCK	I	DIG	SPI clock (Option)
CSB	I	DIG	Chip Select for SPI interface (active low) (Option)
SPIMODE	I	DIG	Enable SPI interface for writing of learning data into array (Option)
SDO	O	DIG	SPI data out (Option)

Remarks: DIG: Digital

6 Interface Access

AI KNN Classification SoftIP & FPGA IP offers two modes for learning data, SPI mode and high speed mode. SPI mode is achieved with pulling pin SPIMODE to logic high, and training data is communicated with AI KNN Classification SoftIP through CSB, SCK and SDI pins. When using high speed mode, SPIMODE is driven to logic low, and training data is communicated through ARRAYWE, 32 bits and 21/20/19 bits ARRAYADDRESS for SoftIP and 19 bits of ARRAYADDRESS for FPGA IP.

6.1 LEARNING DATA THROUGH SPI MODE

The SPI mode allows a low pin count mode of communication between the host controller and AI KNN Classification IP. The SPI mode consists of a simple SPI write from host controller to AI KNN Classification SoftIP using CSB, SDI and SCK. Each cycle of SPI only allows 8 bits of information being transferred, thus to parse the information of address of 19 bits and data of 32 bits, it requires 7 SPI cycles as shown in Figure 3.

SPI mode is optional and may not be needed for most cases as the AI KNN Classification SoftIP is integrated with other logic in an ASIC or SOC, thus allowing direct access to the SoftIP using high speed more.

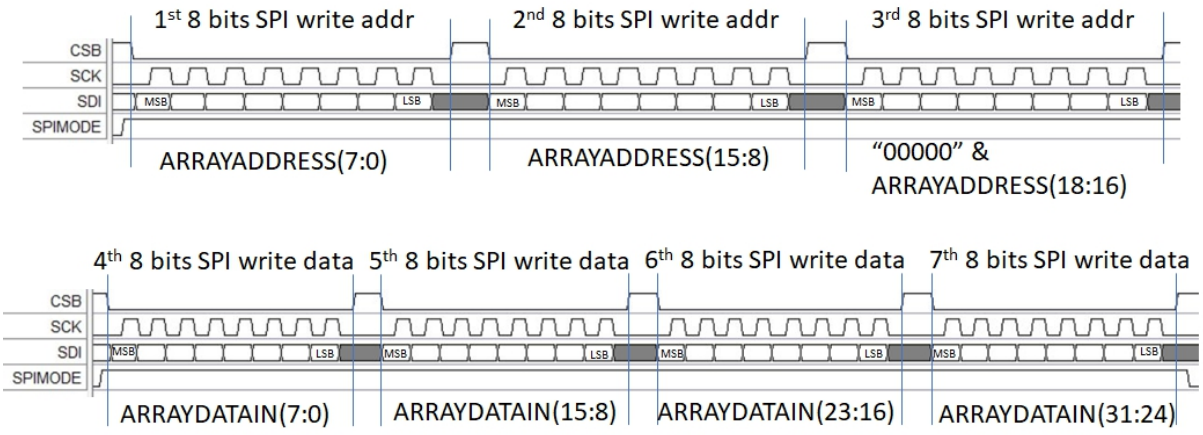


Figure 3. Writing of Learning Data and Classification Data into AI KNN Classifcation SoftIP Using SPI Interface

The SPI mode of communication of writing of learning data and classification data requires fewer signal connections but is slower compared to the high speed mode. SPI is optional and may be removed if not in use.

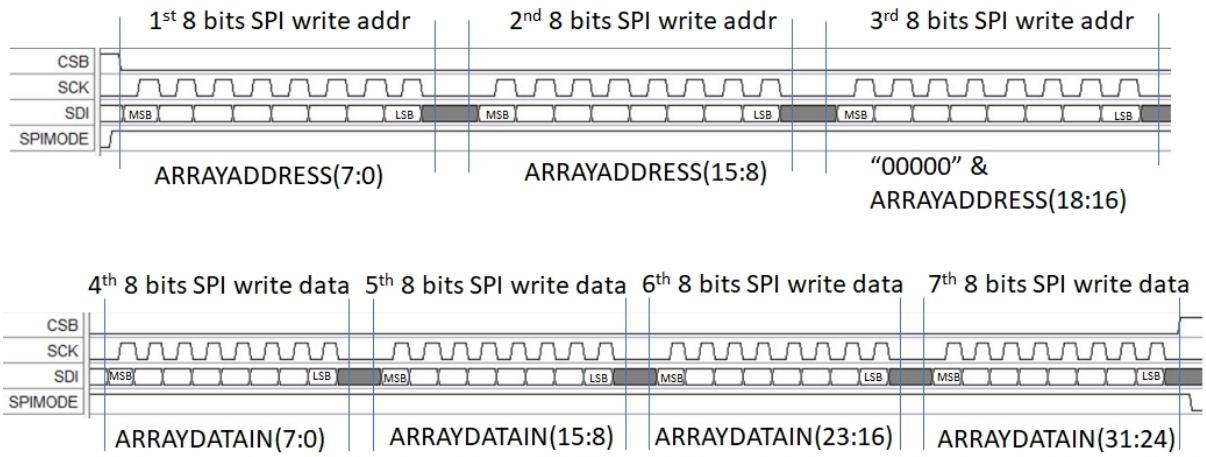


Figure 4. Writing of Learning Data and Classification Data into AI KNN Classification SoftIP Using SPI Interface With CSB Low Throughout Address and Throughout Data

6.2 LEARNING DATA THROUGH HIGH SPEED MODE

The high speed mode is used to write learning data, classification data into AI KNN Classification SoftIP & FPGA IP when SPIMODE is at logic low. The write is a synchronous write at rising edge of clock when ARRAYWE is at logic high. The data from ARRAYDATAIN(31:0) is written into the AI KNN Classification SoftIP at address of ARRAYADDRESS(20/19/18:0) and FPGA IP at address of ARRAYADDRESS(11/10/9:0). The host need to drive more signals as compared to SPI mode, but in high speed mode, the host can write many learning data at a high speed rate, as shown in Figure 5.

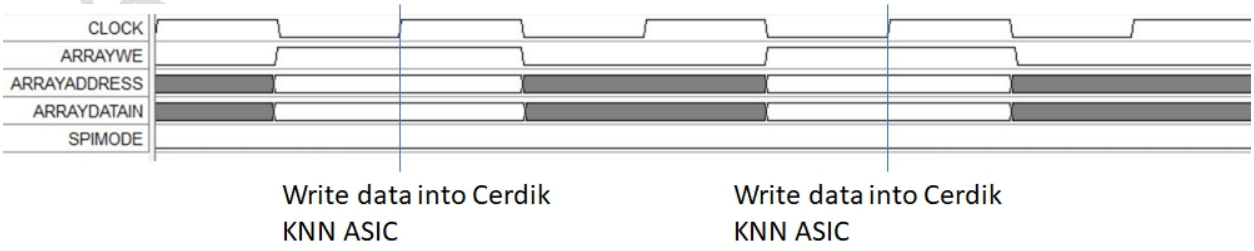


Figure 5. Writing of Learning Data and Classification Data into AI KNN Classification SoftIP Using High Speed Mode

The method of high speed communication is ideally suited when the host have the ability to drive more signals and require a high speed writing of learning data into AI KNN Classification IP.

7 Learning Data

AI KNN Classification SoftIP have a capacity for learning data up to 1024 samples with each sample having up to a maximum of 1024 attributes as shown in Figure 6. The number of samples can vary from 2 samples to 1024 samples and is specified in the ROWSIZE register. Each sample can vary from 64 attributes to 1024 attributes with increments of 64 (64, 128, 192, 256, 320, … 1024) and is specified in the COLUMNSIZE register. Each attribute is represented by a 8 bits data, thus the 32 bits ARRAYDATAIN represent the data for 4 attributes, with the addressing of each attribute shown in Figure 7. The addressing for learning data of maximum 1024 samples with each sample being 1024 attributes is from 0x00000 to 0x3FFFF.

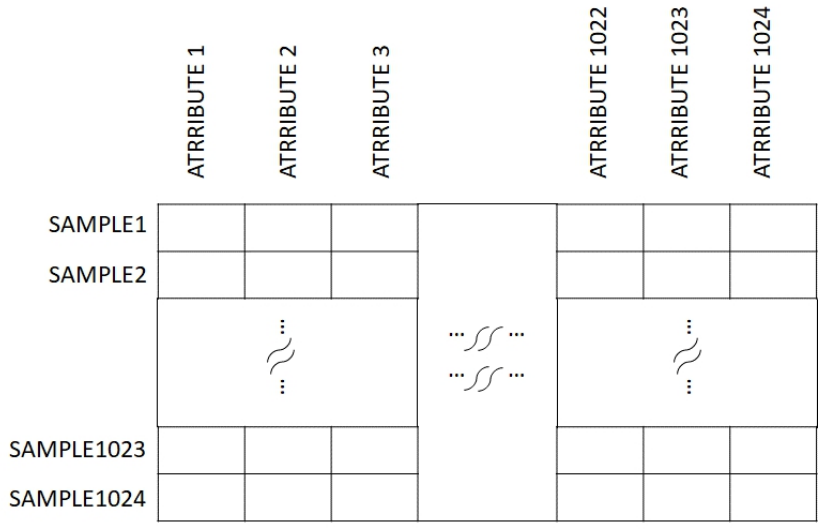


Figure 6. AI KNN Classification SoftIP With 1024 Samples And 1024 Attributes Per Sample

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(18:0)=0x00000	Sample 1, Attribute 1	Sample 1, Attribute 2	Sample 1, Attribute 3	Sample 1, Attribute 4
ARRAYADDRESS(18:0)=0x00001	Sample 1, Attribute 5	Sample 1, Attribute 6	Sample 1, Attribute 7	Sample 1, Attribute 8
ARRAYADDRESS(18:0)=0x00002	Sample 1, Attribute 9	Sample 1, Attribute 10	Sample 1, Attribute 11	Sample 1, Attribute 12
ARRAYADDRESS(18:0)=0x00003	Sample 1, Attribute 13	Sample 1, Attribute 14	Sample 1, Attribute 15	Sample 1, Attribute 16
⋮				
ARRAYADDRESS(18:0)=0x000FC	Sample 1, Attribute 1009	Sample 1, Attribute 1010	Sample 1, Attribute 1011	Sample 1, Attribute 1012
ARRAYADDRESS(18:0)=0x000FD	Sample 1, Attribute 1013	Sample 1, Attribute 1014	Sample 1, Attribute 1015	Sample 1, Attribute 1016
ARRAYADDRESS(18:0)=0x000FE	Sample 1, Attribute 1017	Sample 1, Attribute 1018	Sample 1, Attribute 1019	Sample 1, Attribute 1020
ARRAYADDRESS(18:0)=0x000FF	Sample 1, Attribute 1021	Sample 1, Attribute 1022	Sample 1, Attribute 1023	Sample 1, Attribute 1024
ARRAYADDRESS(18:0)=0x00100	Sample 2, Attribute 1	Sample 2, Attribute 2	Sample 2, Attribute 3	Sample 2, Attribute 4
ARRAYADDRESS(18:0)=0x00101	Sample 2, Attribute 5	Sample 2, Attribute 6	Sample 2, Attribute 7	Sample 2, Attribute 8
ARRAYADDRESS(18:0)=0x00102	Sample 2, Attribute 9	Sample 2, Attribute 10	Sample 2, Attribute 11	Sample 2, Attribute 12
ARRAYADDRESS(18:0)=0x00103	Sample 2, Attribute 13	Sample 2, Attribute 14	Sample 2, Attribute 15	Sample 2, Attribute 16
⋮				
ARRAYADDRESS(18:0)=0x3FFFC	Sample 1024, Attribute 1009	Sample 1024, Attribute 1010	Sample 1024, Attribute 1011	Sample 1024, Attribute 1012
ARRAYADDRESS(18:0)=0x3FFFD	Sample 1024, Attribute 1013	Sample 0241, Attribute 1014	Sample 1024, Attribute 1015	Sample 1024, Attribute 1016
ARRAYADDRESS(18:0)=0x3FFFE	Sample 1024, Attribute 1017	Sample 1024, Attribute 1018	Sample 1024, Attribute 1019	Sample 1024, Attribute 1020
ARRAYADDRESS(18:0)=0x3FFFF	Sample 1024, Attribute 1021	Sample 1024, Attribute 1022	Sample 1024, Attribute 1023	Sample 1024, Attribute 1024

Figure 7. Learning Data Addressing for AI KNN Classification SoftIP for 1 Mbyte Learning Data

FPGA IP have a capacity for learning data up to 1024 samples with each sample having up to a maximum of 1024 attributes, depending on which FPGA option is chosen. The number of samples can vary from 2 samples to 1024 samples and is specified in the ROWSIZE register. Each sample can vary from 64 attributes to 1024 attributes with increments of 64 (64, 128, 192, 256, 320, … 1024) and is specified in the COLUMNSIZE register. Each sample can vary from 64 attributes or 128 attributes depending on which option is chosen. Each attribute is represented by a 8 bits data, thus the 32 bits ARRAYDATAIN represent the data for 4 attributes, with the addressing of each attribute shown in Figure 8. The addressing for learning data of maximum 100 samples with each sample being 128 attributes is from 0x000 to 0xC7F. The addressing for learning data of maximum 100 samples with each sample being 64 attributes is from 0x000 to 0x63F as shown in Figure 9.

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(11:0)=0x000	Sample 1, Attribute 1	Sample 1, Attribute 2	Sample 1, Attribute 3	Sample 1, Attribute 4
ARRAYADDRESS(11:0)=0x001	Sample 1, Attribute 5	Sample 1, Attribute 6	Sample 1, Attribute 7	Sample 1, Attribute 8
ARRAYADDRESS(11:0)=0x002	Sample 1, Attribute 9	Sample 1, Attribute 10	Sample 1, Attribute 11	Sample 1, Attribute 12
ARRAYADDRESS(11:0)=0x003	Sample 1, Attribute 13	Sample 1, Attribute 14	Sample 1, Attribute 15	Sample 1, Attribute 16
⋮				
ARRAYADDRESS(11:0)=0x01F	Sample 1, Attribute 125	Sample 1, Attribute 126	Sample 1, Attribute 127	Sample 1, Attribute 128
ARRAYADDRESS(11:0)=0x020	Sample 2, Attribute 1	Sample 2, Attribute 2	Sample 2, Attribute 3	Sample 2, Attribute 4
ARRAYADDRESS(11:0)=0x021	Sample 2, Attribute 5	Sample 2, Attribute 6	Sample 2, Attribute 7	Sample 2, Attribute 8
ARRAYADDRESS(11:0)=0x022	Sample 2, Attribute 9	Sample 2, Attribute 10	Sample 2, Attribute 11	Sample 2, Attribute 12
ARRAYADDRESS(11:0)=0x023	Sample 2, Attribute 13	Sample 2, Attribute 14	Sample 2, Attribute 15	Sample 2, Attribute 16
ARRAYADDRESS(11:0)=0x024	Sample 2, Attribute 17	Sample 2, Attribute 18	Sample 2, Attribute 19	Sample 2, Attribute 20
ARRAYADDRESS(11:0)=0x025	Sample 2, Attribute 21	Sample 2, Attribute 22	Sample 2, Attribute 23	Sample 2, Attribute 24
ARRAYADDRESS(11:0)=0x026	Sample 2, Attribute 25	Sample 2, Attribute 26	Sample 2, Attribute 27	Sample 2, Attribute 28
⋮				
ARRAYADDRESS(11:0)=0xC7C	Sample 100, Attribute 113	Sample 100, Attribute 114	Sample 100, Attribute 115	Sample 100, Attribute 116
ARRAYADDRESS(11:0)=0xC7D	Sample 100, Attribute 117	Sample 100, Attribute 118	Sample 100, Attribute 119	Sample 100, Attribute 120
ARRAYADDRESS(11:0)=0xC7E	Sample 100, Attribute 121	Sample 100, Attribute 122	Sample 100, Attribute 123	Sample 100, Attribute 124
ARRAYADDRESS(11:0)=0xC7F	Sample 100, Attribute 125	Sample 100, Attribute 126	Sample 100, Attribute 127	Sample 100, Attribute 128

Figure 8. Learning Data Addressing for AI KNN Classification FPGA IP for 12,800 Bytes Learning Data of 100 Samples With 128 Attributes Per Sample

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(10:0)=0x000	Sample 1, Attribute 1	Sample 1, Attribute 2	Sample 1, Attribute 3	Sample 1, Attribute 4
ARRAYADDRESS(10:0)=0x001	Sample 1, Attribute 5	Sample 1, Attribute 6	Sample 1, Attribute 7	Sample 1, Attribute 8
ARRAYADDRESS(10:0)=0x002	Sample 1, Attribute 9	Sample 1, Attribute 10	Sample 1, Attribute 11	Sample 1, Attribute 12
ARRAYADDRESS(10:0)=0x003	Sample 1, Attribute 13	Sample 1, Attribute 14	Sample 1, Attribute 15	Sample 1, Attribute 16
⋮				
ARRAYADDRESS(10:0)=0x00F	Sample 1, Attribute 61	Sample 1, Attribute 62	Sample 1, Attribute 63	Sample 1, Attribute 64
ARRAYADDRESS(10:0)=0x010	Sample 2, Attribute 1	Sample 2, Attribute 2	Sample 2, Attribute 3	Sample 2, Attribute 4
ARRAYADDRESS(10:0)=0x011	Sample 2, Attribute 5	Sample 2, Attribute 6	Sample 2, Attribute 7	Sample 2, Attribute 8
ARRAYADDRESS(10:0)=0x012	Sample 2, Attribute 9	Sample 2, Attribute 10	Sample 2, Attribute 11	Sample 2, Attribute 12
ARRAYADDRESS(10:0)=0x013	Sample 2, Attribute 13	Sample 2, Attribute 14	Sample 2, Attribute 15	Sample 2, Attribute 16
ARRAYADDRESS(10:0)=0x014	Sample 2, Attribute 17	Sample 2, Attribute 18	Sample 2, Attribute 19	Sample 2, Attribute 20
ARRAYADDRESS(10:0)=0x015	Sample 2, Attribute 21	Sample 2, Attribute 22	Sample 2, Attribute 23	Sample 2, Attribute 24
ARRAYADDRESS(10:0)=0x016	Sample 2, Attribute 25	Sample 2, Attribute 26	Sample 2, Attribute 27	Sample 2, Attribute 28
⋮				
ARRAYADDRESS(10:0)=0x63C	Sample 100, Attribute 49	Sample 100, Attribute 50	Sample 100, Attribute 51	Sample 100, Attribute 52
ARRAYADDRESS(10:0)=0x63D	Sample 100, Attribute 53	Sample 100, Attribute 54	Sample 100, Attribute 55	Sample 100, Attribute 56
ARRAYADDRESS(10:0)=0x63E	Sample 100, Attribute 57	Sample 100, Attribute 58	Sample 100, Attribute 59	Sample 100, Attribute 60
ARRAYADDRESS(10:0)=0x63F	Sample 100, Attribute 61	Sample 100, Attribute 62	Sample 100, Attribute 63	Sample 100, Attribute 64

Figure 9. Learning Data Addressing for AI KNN Classification FPGA IP for 6,400 Bytes Learning Data of 100 Samples With 64 Attributes Per Sample

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(10:0)=0x000	Sample 1, Attribute 1	Sample 1, Attribute 2	Sample 1, Attribute 3	Sample 1, Attribute 4
ARRAYADDRESS(10:0)=0x001	Sample 1, Attribute 5	Sample 1, Attribute 6	Sample 1, Attribute 7	Sample 1, Attribute 8
ARRAYADDRESS(10:0)=0x002	Sample 1, Attribute 9	Sample 1, Attribute 10	Sample 1, Attribute 11	Sample 1, Attribute 12
ARRAYADDRESS(10:0)=0x003	Sample 1, Attribute 13	Sample 1, Attribute 14	Sample 1, Attribute 15	Sample 1, Attribute 16
⋮				
ARRAYADDRESS(10:0)=0x01F	Sample 1, Attribute 125	Sample 1, Attribute 126	Sample 1, Attribute 127	Sample 1, Attribute 128
ARRAYADDRESS(10:0)=0x020	Sample 2, Attribute 1	Sample 2, Attribute 2	Sample 2, Attribute 3	Sample 2, Attribute 4
ARRAYADDRESS(10:0)=0x021	Sample 2, Attribute 5	Sample 2, Attribute 6	Sample 2, Attribute 7	Sample 2, Attribute 8
ARRAYADDRESS(10:0)=0x022	Sample 2, Attribute 9	Sample 2, Attribute 10	Sample 2, Attribute 11	Sample 2, Attribute 12
ARRAYADDRESS(10:0)=0x023	Sample 2, Attribute 13	Sample 2, Attribute 14	Sample 2, Attribute 15	Sample 2, Attribute 16
ARRAYADDRESS(10:0)=0x024	Sample 2, Attribute 17	Sample 2, Attribute 18	Sample 2, Attribute 19	Sample 2, Attribute 20
ARRAYADDRESS(10:0)=0x025	Sample 2, Attribute 21	Sample 2, Attribute 22	Sample 2, Attribute 23	Sample 2, Attribute 24
ARRAYADDRESS(10:0)=0x026	Sample 2, Attribute 25	Sample 2, Attribute 26	Sample 2, Attribute 27	Sample 2, Attribute 28
⋮				
ARRAYADDRESS(10:0)=0x63C	Sample 50, Attribute 113	Sample 50, Attribute 114	Sample 50, Attribute 115	Sample 50, Attribute 116
ARRAYADDRESS(10:0)=0x63D	Sample 50, Attribute 117	Sample 50, Attribute 118	Sample 50, Attribute 119	Sample 50, Attribute 120
ARRAYADDRESS(10:0)=0x63E	Sample 50, Attribute 121	Sample 50, Attribute 122	Sample 50, Attribute 123	Sample 50, Attribute 124
ARRAYADDRESS(10:0)=0x63F	Sample 50, Attribute 125	Sample 50, Attribute 126	Sample 50, Attribute 127	Sample 50, Attribute 128

Figure 10. Learning Data Addressing for AI KNN Classification FPGA IP for 6,400 Bytes Learning Data of 50 Samples With 128 Attributes Per Sample

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(9:0)=0x000	Sample 1, Attribute 1	Sample 1, Attribute 2	Sample 1, Attribute 3	Sample 1, Attribute 4
ARRAYADDRESS(9:0)=0x001	Sample 1, Attribute 5	Sample 1, Attribute 6	Sample 1, Attribute 7	Sample 1, Attribute 8
ARRAYADDRESS(9:0)=0x002	Sample 1, Attribute 9	Sample 1, Attribute 10	Sample 1, Attribute 11	Sample 1, Attribute 12
ARRAYADDRESS(9:0)=0x003	Sample 1, Attribute 13	Sample 1, Attribute 14	Sample 1, Attribute 15	Sample 1, Attribute 16
⋮				
ARRAYADDRESS(9:0)=0x00F	Sample 1, Attribute 61	Sample 1, Attribute 62	Sample 1, Attribute 63	Sample 1, Attribute 64
ARRAYADDRESS(9:0)=0x010	Sample 2, Attribute 1	Sample 2, Attribute 2	Sample 2, Attribute 3	Sample 2, Attribute 4
ARRAYADDRESS(9:0)=0x011	Sample 2, Attribute 5	Sample 2, Attribute 6	Sample 2, Attribute 7	Sample 2, Attribute 8
ARRAYADDRESS(9:0)=0x012	Sample 2, Attribute 9	Sample 2, Attribute 10	Sample 2, Attribute 11	Sample 2, Attribute 12
ARRAYADDRESS(9:0)=0x013	Sample 2, Attribute 13	Sample 2, Attribute 14	Sample 2, Attribute 15	Sample 2, Attribute 16
ARRAYADDRESS(9:0)=0x014	Sample 2, Attribute 17	Sample 2, Attribute 18	Sample 2, Attribute 19	Sample 2, Attribute 20
ARRAYADDRESS(9:0)=0x015	Sample 2, Attribute 21	Sample 2, Attribute 22	Sample 2, Attribute 23	Sample 2, Attribute 24
ARRAYADDRESS(9:0)=0x016	Sample 2, Attribute 25	Sample 2, Attribute 26	Sample 2, Attribute 27	Sample 2, Attribute 28
⋮				
ARRAYADDRESS(9:0)=0x31C	Sample 50, Attribute 49	Sample 50, Attribute 50	Sample 50, Attribute 51	Sample 50, Attribute 52
ARRAYADDRESS(9:0)=0x31D	Sample 50, Attribute 53	Sample 50, Attribute 54	Sample 50, Attribute 55	Sample 50, Attribute 56
ARRAYADDRESS(9:0)=0x31E	Sample 50, Attribute 57	Sample 50, Attribute 58	Sample 50, Attribute 59	Sample 50, Attribute 60
ARRAYADDRESS(9:0)=0x31F	Sample 50, Attribute 61	Sample 50, Attribute 62	Sample 50, Attribute 63	Sample 50, Attribute 64

Figure 11. Learning Data Addressing for AI KNN Classification FPGA IP for 3,200 Bytes Learning Data of 50 Samples With 64 Attributes Per Sample

8 Array Class Data

Each learning data sample have an array class associated with it. It is represented by an 8 bit data with address from 40000 hex to 403FF hex for SoftIP of 1 Mbyte option as shown in Figure 12. The contents of Array Class Data is limited to a value of 00 hex to 1F hex as shown in Figure 17. For large learning data classes, an Array Class Data of up to 256 is possible using SPI option (please contact Airis Labs on usage of this extended array class for large learning data classes).

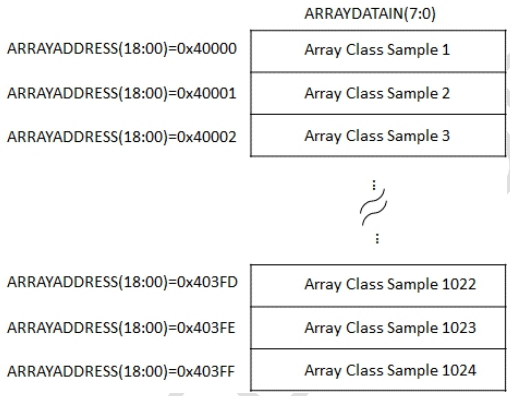


Figure 12. Array Class Data Addressing for AI KNN Classification Soft IP for 1 Mbyte Learning Data

For FPGA IP with 12,800 bytes of learning data for 100 samples of 128 attributes per sample of learning data, address for array class range from C80 hex to CE3 hex as shown in Figure 13.

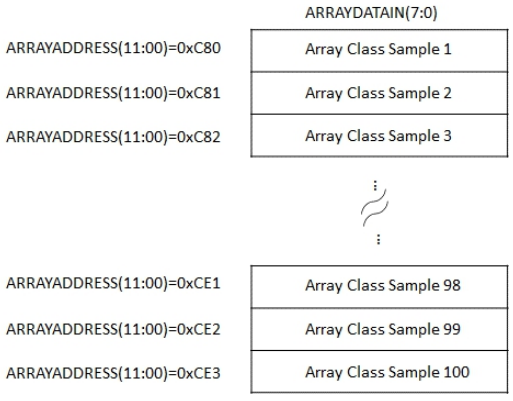


Figure 13. Array Class Data Addressing for AI KNN Classification FPGA IP for 12,800 Bytes of Learning Data

For FPGA IP with 6,400 bytes of learning data for 100 samples of 64 attributes per sample of learning data, address for array class range from 640 hex to 6A3 hex as shown in Figure 14.

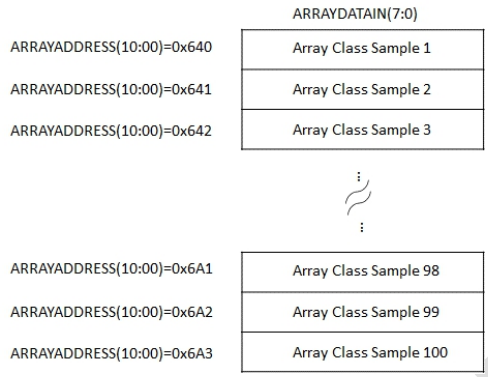


Figure 14. Array Class Data Addressing for AI KNN Classification FPGA IP for 6,400 Bytes of Learning Data of 100 Samples With 64 Attributes Per Sample

For FPGA IP with 6,400 bytes of learning data for 50 samples of 128 attributes per sample of learning data, address for array class range from 640 hex to 671 hex as shown in Figure 15.

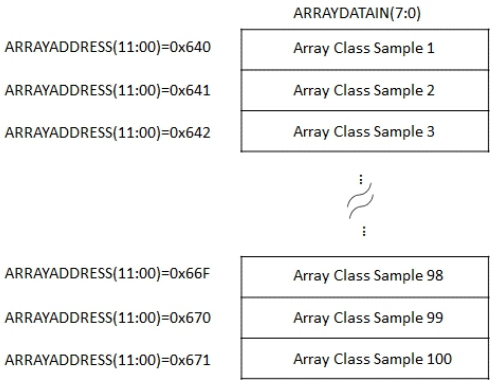


Figure 15. Array Class Data Addressing for AI KNN Classification FPGA IP for 6,400 Bytes of Learning Data of 50 Samples With 128 Attributes Per Sample

For FPGA IP with 3,200 bytes of learning data for 50 samples of 64 attributes per sample of learning data, address for array class range from 320 hex to 351 hex as shown in Figure 16.

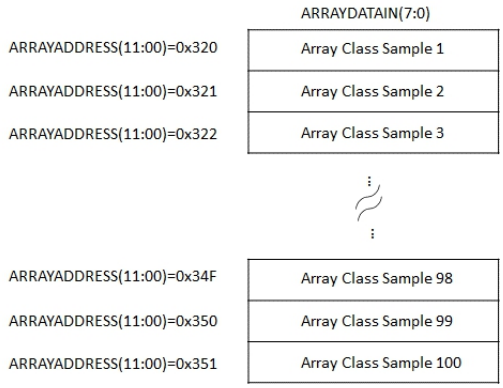


Figure 16. Array Class Data Addressing for AI KNN Classification FPGA IP for 3,200 Bytes of Learning Data

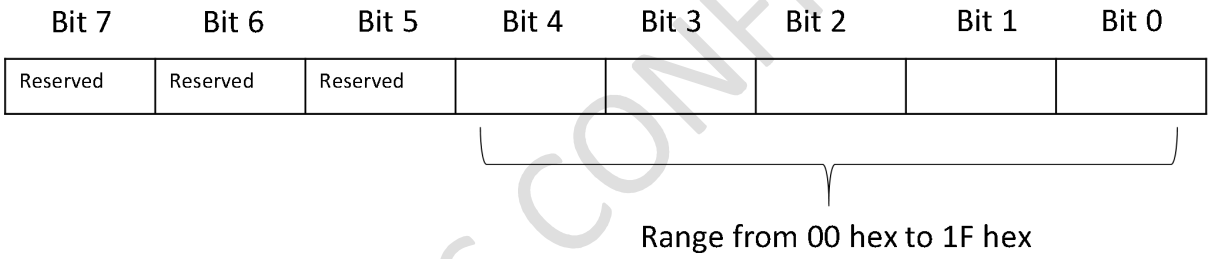


Figure 17. Array Class Data Range from 00 Hex to 1F Hex

9 Classification Test Data

Classification test data is the data entered into AI KNN Classification SoftIP for the KNN algorithm to determine which array class it is closest to based on the input value of K(3:0). The Classification test data have the addressing from 7FF00 Hex to 7FFFF Hex for SoftIP with 1 Mbyte learning data as shown in Figure 18.

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(18:0)=0x7FF00	Classification Test Attribute 1	Classification Test Attribute 2	Classification Test Attribute 3	Classification Test Attribute 4
ARRAYADDRESS(18:0)=0x7FF01	Classification Test Attribute 5	Classification Test Attribute 6	Classification Test Attribute 7	Classification Test Attribute 8
ARRAYADDRESS(18:0)=0x7FF02	Classification Test Attribute 9	Classification Test Attribute 10	Classification Test Attribute 11	Classification Test Attribute 12
ARRAYADDRESS(18:0)=0x7FF03	Classification Test Attribute 13	Classification Test Attribute 14	Classification Test Attribute 15	Classification Test Attribute 16
⋮				
ARRAYADDRESS(18:0)=0x7FFFC	Classification Test Attribute 1009	Classification Test Attribute 1010	Classification Test Attribute 1011	Classification Test Attribute 1012
ARRAYADDRESS(18:0)=0x7FFFD	Classification Test Attribute 1013	Classification Test Attribute 1014	Classification Test Attribute 1015	Classification Test Attribute 1016
ARRAYADDRESS(18:0)=0x7FFFE	Classification Test Attribute 1017	Classification Test Attribute 1018	Classification Test Attribute 1019	Classification Test Attribute 1020
ARRAYADDRESS(18:0)=0x7FFFF	Classification Test Attribute 1021	Classification Test Attribute 1022	Classification Test Attribute 1023	Classification Test Attribute 1024

Figure 18. Classification Test Data Addressing for AI KNN Classification SoftIP for 1 Mbyte Learning Data

For FPGA IP with 12,800 bytes learning data, classification test data have the addressing from FE0 Hex to FFF Hex as shown in Figure 19.

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(11:0)=0xFE0	Classification Test Attribute 1	Classification Test Attribute 2	Classification Test Attribute 3	Classification Test Attribute 4
ARRAYADDRESS(11:0)=0xFE1	Classification Test Attribute 5	Classification Test Attribute 6	Classification Test Attribute 7	Classification Test Attribute 8
ARRAYADDRESS(11:0)=0xFE2	Classification Test Attribute 9	Classification Test Attribute 10	Classification Test Attribute 11	Classification Test Attribute 12
ARRAYADDRESS(11:0)=0xFE3	Classification Test Attribute 13	Classification Test Attribute 14	Classification Test Attribute 15	Classification Test Attribute 16
⋮				
ARRAYADDRESS(11:0)=0xFFC	Classification Test Attribute 113	Classification Test Attribute 114	Classification Test Attribute 115	Classification Test Attribute 116
ARRAYADDRESS(11:0)=0xFFD	Classification Test Attribute 117	Classification Test Attribute 118	Classification Test Attribute 119	Classification Test Attribute 120
ARRAYADDRESS(11:0)=0xFFE	Classification Test Attribute 121	Classification Test Attribute 122	Classification Test Attribute 123	Classification Test Attribute 124
ARRAYADDRESS(11:0)=0xFFF	Classification Test Attribute 125	Classification Test Attribute 126	Classification Test Attribute 127	Classification Test Attribute 128

Figure 19. Classification Test Data Addressing for AI KNN Classification FPGA IP for 12,800 Bytes of Learning Data

For FPGA IP with 6,400 bytes learning data of 100 Samples with 64 attributes per sample, classification test data have the addressing from 7F0 Hex to 7FF Hex as shown in Figure 20.

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(10:0)=0x7F0	Classification Test Attribute 1	Classification Test Attribute 2	Classification Test Attribute 3	Classification Test Attribute 4
ARRAYADDRESS(10:0)=0x7F1	Classification Test Attribute 5	Classification Test Attribute 6	Classification Test Attribute 7	Classification Test Attribute 8
ARRAYADDRESS(10:0)=0x7F2	Classification Test Attribute 9	Classification Test Attribute 10	Classification Test Attribute 11	Classification Test Attribute 12
ARRAYADDRESS(10:0)=0x7F3	Classification Test Attribute 13	Classification Test Attribute 14	Classification Test Attribute 15	Classification Test Attribute 16
⋮				
ARRAYADDRESS(10:0)=0x7FC	Classification Test Attribute 49	Classification Test Attribute 50	Classification Test Attribute 51	Classification Test Attribute 52
ARRAYADDRESS(10:0)=0x7FD	Classification Test Attribute 53	Classification Test Attribute 54	Classification Test Attribute 55	Classification Test Attribute 56
ARRAYADDRESS(10:0)=0x7FE	Classification Test Attribute 57	Classification Test Attribute 58	Classification Test Attribute 59	Classification Test Attribute 60
ARRAYADDRESS(10:0)=0x7FF	Classification Test Attribute 61	Classification Test Attribute 62	Classification Test Attribute 63	Classification Test Attribute 64

Figure 20. Classification Test Data Addressing for AI KNN Classification FPGA IP for 6,400 Bytes of Learning Data for 100 Samples With 64 Attributes Per Sample

For FPGA IP with 6,400 bytes learning data of 50 Samples with 128 attributes per sample, classification test data have the addressing from 7E0 Hex to 7FF Hex as shown in Figure 21.

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(10:0)=0x7E0	Classification Test Attribute 1	Classification Test Attribute 2	Classification Test Attribute 3	Classification Test Attribute 4
ARRAYADDRESS(10:0)=0x7E1	Classification Test Attribute 5	Classification Test Attribute 6	Classification Test Attribute 7	Classification Test Attribute 8
ARRAYADDRESS(10:0)=0x7E2	Classification Test Attribute 9	Classification Test Attribute 10	Classification Test Attribute 11	Classification Test Attribute 12
ARRAYADDRESS(10:0)=0x7E3	Classification Test Attribute 13	Classification Test Attribute 14	Classification Test Attribute 15	Classification Test Attribute 16
⋮				
ARRAYADDRESS(10:0)=0x7FC	Classification Test Attribute 113	Classification Test Attribute 114	Classification Test Attribute 115	Classification Test Attribute 116
ARRAYADDRESS(10:0)=0x7FD	Classification Test Attribute 117	Classification Test Attribute 118	Classification Test Attribute 119	Classification Test Attribute 120
ARRAYADDRESS(10:0)=0x7FE	Classification Test Attribute 121	Classification Test Attribute 122	Classification Test Attribute 123	Classification Test Attribute 124
ARRAYADDRESS(10:0)=0x7FF	Classification Test Attribute 125	Classification Test Attribute 126	Classification Test Attribute 127	Classification Test Attribute 128

Figure 21. Classification Test Data Addressing for AI KNN Classification FPGA IP for 6,400 Bytes of Learning Data for 50 Samples With 128 Attributes Per Sample

For FPGA IP with 3,200 bytes learning data of 50 Samples with 64 attributes per sample, classification test data have the addressing from 3F0 Hex to 3FF Hex as shown in Figure 22.

	ARRAYDATAIN(7:0)	ARRAYDATAIN(15:8)	ARRAYDATAIN(23:16)	ARRAYDATAIN(31:24)
ARRAYADDRESS(9:0)=0x3F0	Classification Test Attribute 1	Classification Test Attribute 2	Classification Test Attribute 3	Classification Test Attribute 4
ARRAYADDRESS(9:0)=0x3F1	Classification Test Attribute 5	Classification Test Attribute 6	Classification Test Attribute 7	Classification Test Attribute 8
ARRAYADDRESS(9:0)=0x3F2	Classification Test Attribute 9	Classification Test Attribute 10	Classification Test Attribute 11	Classification Test Attribute 12
ARRAYADDRESS(9:0)=0x3F3	Classification Test Attribute 13	Classification Test Attribute 14	Classification Test Attribute 15	Classification Test Attribute 16
⋮				
ARRAYADDRESS(9:0)=0x3FC	Classification Test Attribute 49	Classification Test Attribute 50	Classification Test Attribute 51	Classification Test Attribute 52
ARRAYADDRESS(9:0)=0x3FD	Classification Test Attribute 53	Classification Test Attribute 54	Classification Test Attribute 55	Classification Test Attribute 56
ARRAYADDRESS(9:0)=0x3FE	Classification Test Attribute 57	Classification Test Attribute 58	Classification Test Attribute 59	Classification Test Attribute 60
ARRAYADDRESS(9:0)=0x3FF	Classification Test Attribute 61	Classification Test Attribute 62	Classification Test Attribute 63	Classification Test Attribute 64

Figure 22. Classification Test Data Addressing for AI KNN Classification FPGA IP for 3,200 Bytes of Learning Data for 50 Samples With 64 Attributes Per Sample

10 Configuration Registers

AI KNN Classification SoftIP have three configuration registers that the user can use to configure the KNN functionality.

Table 1. Configuration Registers for AI KNN Classification SoftIP for 1 Mbyte Learning Data

Address (Hex)	Register Name	Register Size
7FEFC	Threshold	32 bits
7FEFD	Distance Type	8 bits
7FEFE	Row Size	11 bits
7FEFF	Column Size	11 bits (Must be multiples of 64 either 64, 128, 192, 256, 320, 384, 448, 512, 576, 640, 704, 768, 832, 896, 960, 1024)

Table 2. Configuration Registers for AI KNN Classification FPGA IP for 12,800 Bytes Learning Data of 100 Samples With 128 Attributes Per Sample

Address (Hex)	Register Name	Register Size
FDC	Threshold	32 bits
FDD	Distance Type	8 bits
FDE	Row Size	7 bits (value of 2 to 100)
FDF	Column Size	7 bits (value of 64 or 128)

Table 3. Configuration Registers for AI KNN Classification FPGA IP for 6,400 Bytes Learning Data of 100 Samples With 64 Attributes Per Sample

Address (Hex)	Register Name	Register Size
7EC	Threshold	32 bits
7ED	Distance Type	8 bits

7EE	Row Size	7 bits (value of 2 to 100)
7EF	Column Size	7 bits (value of 64 only)

Table 4. Configuration Registers for AI KNN Classification FPGA IP for 6,400 Bytes Learning Data of 50 Samples With 128 Attributes Per Sample

Address (Hex)	Register Name	Register Size
7DC	Threshold	32 bits
7DD	Distance Type	8 bits
7DE	Row Size	7 bits (value of 2 to 50)
7DF	Column Size	7 bits (value of 64 or 128)

Table 5. Configuration Registers for AI KNN Classification FPGA IP for 3,200 Bytes Learning Data of 50 Samples With 64 Attributes Per Sample

Address (Hex)	Register Name	Register Size
3EC	Threshold	32 bits
3ED	Distance Type	8 bits
3EE	Row Size	7 bits (value of 2 to 50)
3EF	Column Size	7 bits (value of 64 only)

10.1 Configuration Registers Description

10.1.1 Threshold Register

Threshold register is a 32 bits register that is used to determine if the calculated output sortarrayclasscount is valid or invalid (all zeros). If the distance value of the calculated nearest neighbor is less than the value of the threshold register, the output sortarrayclasscount is valid, otherwise sortarrayclasscount is invalid with "00000". The threshold register upon reset defaults to 0xFFFFFFFF.

10.1.2 Distance Type Register

Distance Type Register is the register that defines the type of calculation for the distance between the learning data and the classification data.

Register Value (8 Bits Binary)	Functionality
00000000	Euclidean Distance
00000001	Manhattan Distance
00000010	Hamming Distance
00000011 to 11111111	Not Used

Euclidean distance calculation $\sqrt{\sum_{i=1}^{k}(x_i - y_i)^2}$

Manhattan distance calculation $\sum_{i=1}^{k}|x_i - y_i|$

Hamming distance calculation $\sum_{i=i}^{k} D_i$ whereby $D_i = 0$ if $x = y$ else $D_i = 1$ if $x \neq y$

10.1.3 Row Size Register (7FEFE Hex)

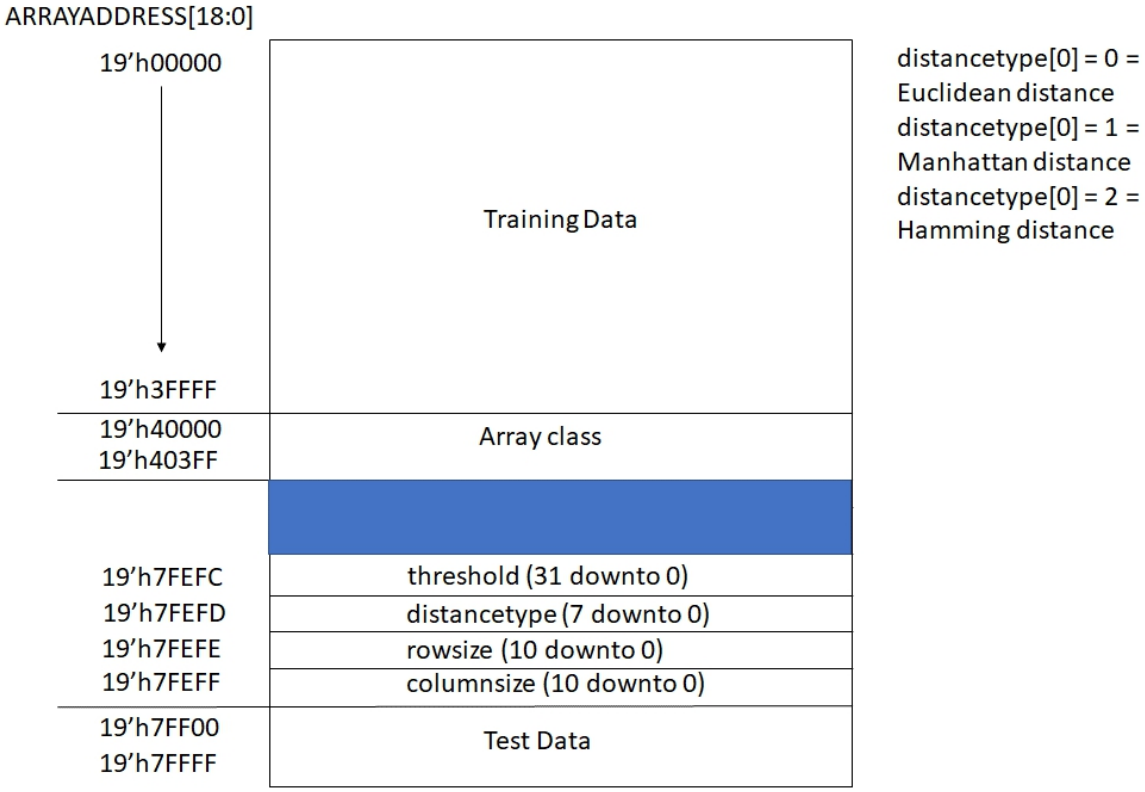
Row Size Register is the register that defines the number of samples in the learning data. It can be a value from 2 to a maximum of 1024.

10.1.4 Column Size Register

Column Size Register is the register that defines the number of attributes per sample in the learning data for SoftIP. It must be a value in multiples of 64 starting from 64 to either 128, 192, 256, 320, 384, 448, 512, 576, 640, 704, 768, 832, 896, 960, 1024. Any other values entered will be invalid.

For FPGA IP, the value is dependent on the option chosen. For example, for FPGA option of 128 attributes, the Column Size Register value is 64 or 128. For FPGA option of 256 attributes, the Column Register value is 64/128/192/256 in multiples of 64.

11AI KNN Classification SoftIP Memory MAP



12 STARTKNN

Once the learning data, array class data, classification test data, row size register, column size register, distance type register have its data input into AI KNN Classification IP, the next step would be to drive the STARTKNN to logic high to start the computations to determine the correlation of the array class data to its nearest neighbor through the array class identifier.

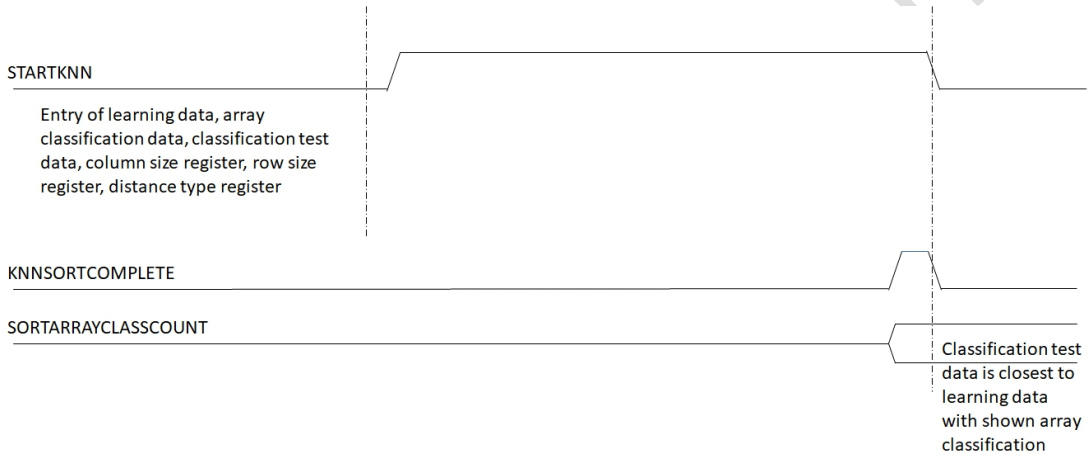


Figure 23. STARTKNN Process to Identify Array Class for Classification Test Data by AI KNN Classification IP

For subsequent KNN classification, STARTKNN is deasserted low once KNNSORTCOMPLETE goes high and the classification result on SORTARRAYCLASSCOUNT is used by the system. The system can re-write a new set of classification test data and distance type register if the system wants to change the method of distance calculation, and reassert STARTKNN to begin the new KNN classification.

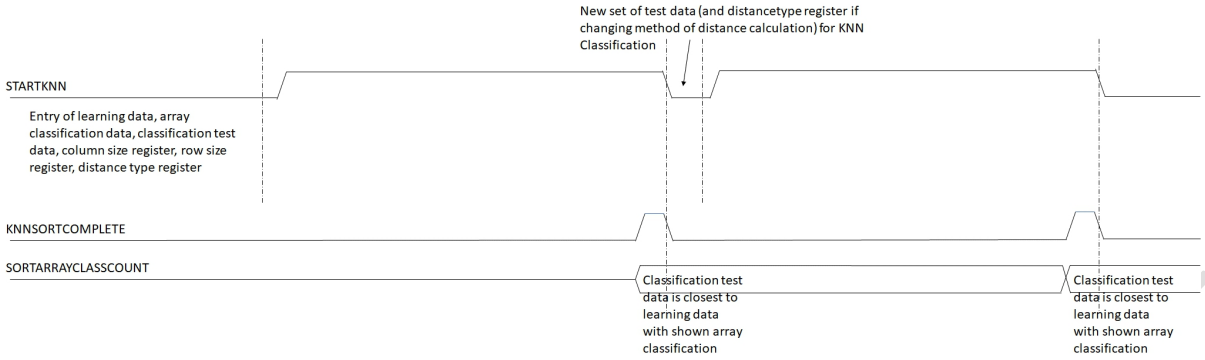


Figure 24. STARTKNN Process to Identify Array Class for Classification Test Data by AI KNN Classification IP

When KNNSORTCOMPLETE goes high and SORTARRAYCLASSCOUNT is valid, the user can change the value of K from 1 to 15. Each time K is changed, the KNN voting is counted again and the results of SORTARRAYCLASSCOUNT is valid after two clock cycles.